REV:A0

LPWSAA3(4)1-MxxC

400G QSFP-DD to 400G QSFP-DD Active Optical Cable

Product Features

- Supports 400Gb/s aggregate bit rate
- 400GAUI-8 Electrical interface aligned with IEEE 802.3bs
- 8x 50Gb/s PAM4 modulation
- maximum cable length upto 60m assembling OM3 multimode fiber
- maximum cable length upto 100m assembling OM4 multimode fiber
- Hot-pluggable QSFP-DD footprint
- +3.3V single power supply
- Low power Consumption,≤8w ,each end
- RoHS-6 compliant and lead-free
- Support Digital Diagnostic Monitor interface
- Case operating temperature Commercial: 0°C to +70°C

Applications

- 400GAUI-8
- Other 400G optical links

Ordering information

Part No. Note1	Cable Bit Rate (Gbps)	Packag form of two opposite sides	Cable lengths	Fiber Type	Temp Note2
LPWSAA**3**1-MXX$_1$C	400G to 400G	QSFP-DD to QSFP-DD	0.5~60m	OM3 MMF	0℃~+70℃
LPWSAA**4**1-MXX$_1$C			0.5~100m	OM4 MMF	
note1 : The "M$_1$XX$_2$" means : ①"XX"= 01~99 ② MXX = XX*1meter; SXX = XX*10meter ; LXX = XX*0.1meter note2: case temperature					

I. Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Ref.
Storage Temperature	T_S	-40		85	ºC	
Storage Ambient Humidity	H_A	0		85	%	
Maximum Supply Voltage	V_{CC}	-0.5		3.6	V	

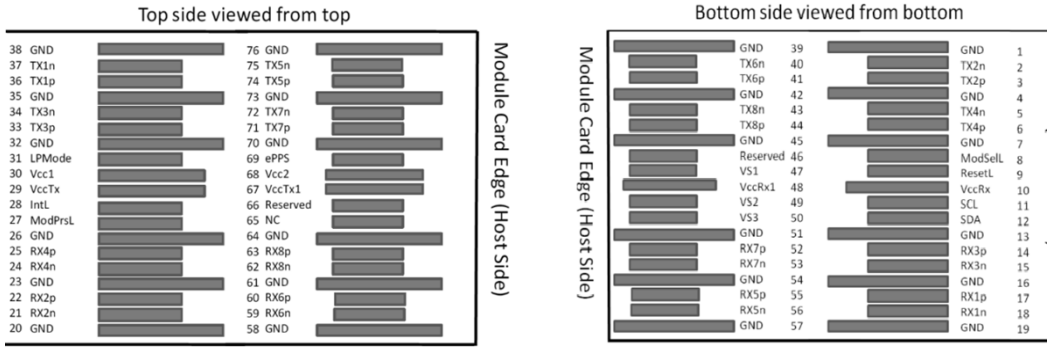
II. Recommended Operating Conditions

Data Rate Specifications	Symbol	Min.	Typ.	Max.	Unit	Ref.
Supply Voltage	Vcc	3.13	3.3	3.47	V	
Baud Rate(per channel)	BR		26.5625		GBd	PAM4
Operating Case Temperature	Tc	0		70	℃	

III. Electrical Interface Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Ref.
Supply Voltage	V_{CC}	3.15		3.45	V	
Power Dissipation （each end）	Pd			10	W	
Transmitter(per Lane)						
Input different impedance	R_{in}	90	100	110	Ω	
Single ended input voltage tolerance	VinT	-0.3		4.0	V	
Differential Input Voltage Amplitude	$V_{in,pp}$			900	mV	
Receiver (per Lane)						
Error Bit Rate	BER			2.4E-4		
Output different impedance	R_{out}	90	100	110	Ω	
Single-ended output voltage	VoutR	-0.3		4.0	V	
Differential Output Voltage Amplitude	$V_{out,pp}$			900	mV	

IV. Pin Diagram

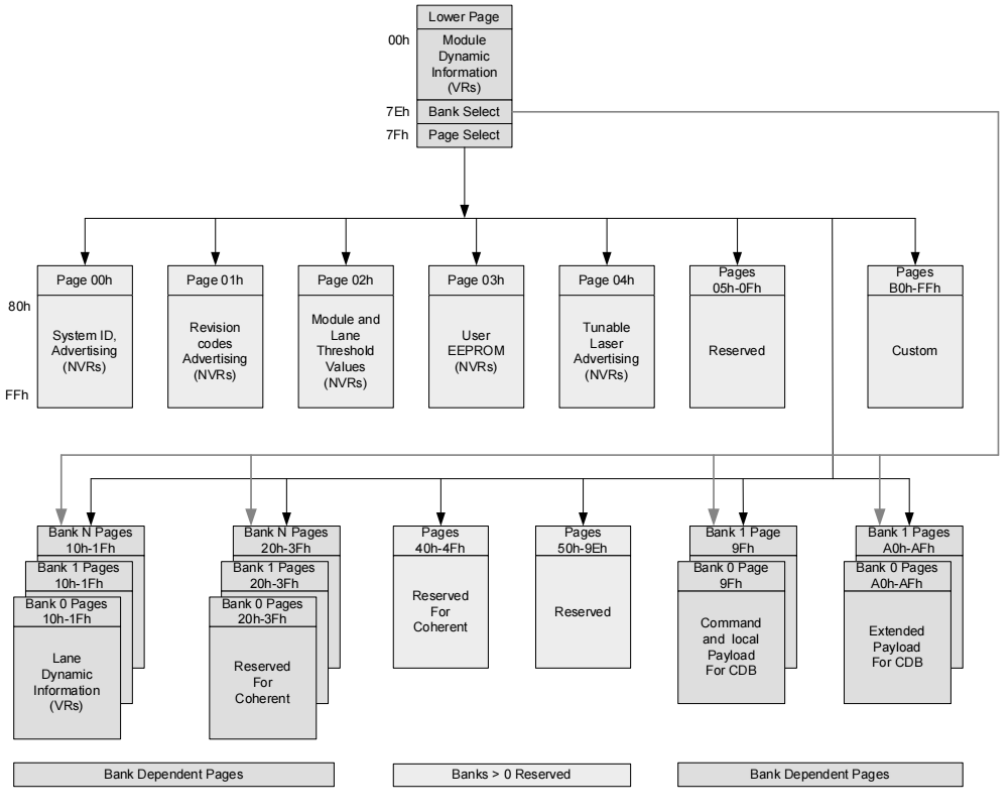


Pin Descriptions for QSFP-DD:

Pin NO.	Logic	Symbol	Definition	PinNO.	Logic	Symbol	Definition
1		GND	Ground	39		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input	40	CML-I	Tx6n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	41	CML-I	Tx6p	Transmitter Non-inverted Data Input
4		GND	Ground	42		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input	43	CML-I	Tx8n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	44	CML-I	Tx8p	Transmitter Non-inverted Data Input
7		GND	Ground	45		GND	Ground
8	LVTTL-I	ModSelL	Module Select	46		Reserved	
9	LVTTL-I	ResetL	Module Reset	47		VS1	Module Vendor Specific 1
10		VccRx	+3.3V Power Supply Receiver	48		VccRx1	3.3V Power Supply
11	LVCMOS-I/O	SCL	2-wire serial interface clock	49		VS2	Module Vendor Specific 2
12	LVCMOS-I/O	SDA	2-wire serial interface data	50		VS3	Module Vendor Specific 3
13		GND	Ground	51		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output	52	CML-O	Rx7p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output	53	CML-O	Rx7n	Receiver Inverted Data Output
16		GND	Ground	54		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output	55	CML-O	Rx5p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output	56	CML-O	Rx5n	Receiver Inverted Data Output
19		GND	Ground	57		GND	Ground
20		GND	Ground	58		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output	59	CML-O	Rx6n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output	60	CML-O	Rx6p	Receiver Non-inverted Data Output
23		GND	Ground	61		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output	62	CML-O	Rx8n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output	63	CML-O	Rx8p	Receiver Non-inverted Data Output
26		GND	Ground	64		GND	Ground
27	LVTTL-O	ModPrsL	Module Present	65		NC	Not connected
28	LVTTL-O	IntL	Interrupt	66		Reserved	
29		VccTx	+3.3V Power Supply Transmitter	67		VccTx1	3.3V Power Supply
30		Vcc1	+3.3V Power Supply	68		Vcc2	3.3V Power Supply
31	LVTTL-I	InitMode	Initialization mode	69		Reserved	
32		GND	Ground	70		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	71	CML-I	Tx7p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input	72	CML-I	Tx7n	Transmitter Inverted Data Input
35		GND	Ground	73		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	74	CML-I	Tx5p	Transmitter Non-inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input	75	CML-I	Tx5n	Transmitter Inverted Data Input
38		GND	Ground	76		GND	Ground

V. Digital Diagnostic Functions

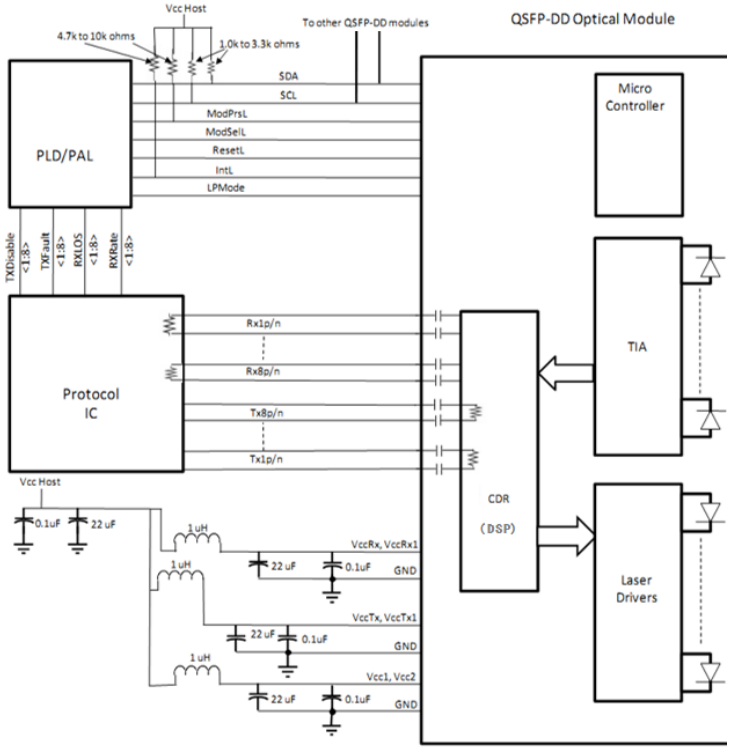
Compatible with QSFP-DD CMIS rev 4.0.



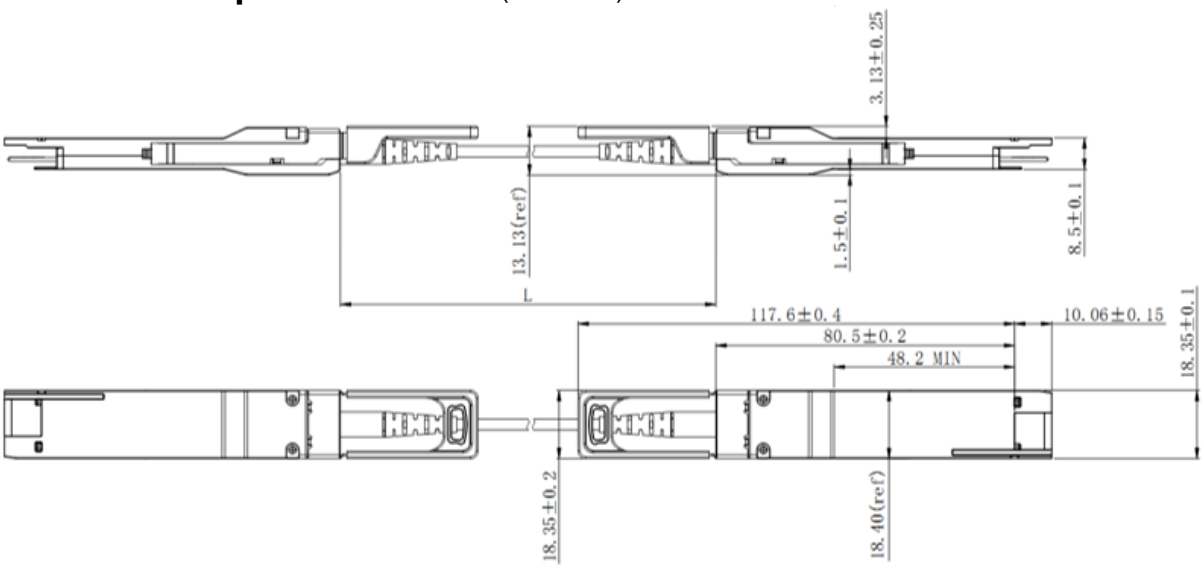
VI. Digital Diagnostic Specification

Parameter	Accuracy	Unit
Internally Measured Transceiver Temperature	+/-3	℃
Internally Measured Transceiver Supply Voltage	+/-3	%
Measured Tx Bias Current	+/-10	%
Measured Tx Output Power	+/-3	dB
Measured Rx Received Average Optical Power	+/-3	dB

VII. Recommended Interface Circuit



VIII. Mechanical Specifications (Unit: mm)



Cable Length (Unit: m)	Tolerant (Unit: cm)
1.0~4.9	+15/-0
5.0~14.9	+30/-0
≥15.0	+2%/-0