LPXWHB31-S50C

OSFP, 800G DR8, 2*MPO-12, 1310nm SMF 500m

Features

- 8x106.25 Gbps electrical interface
- Silicon photonics integrated solution
- Hot-pluggable OSFP form factor
- Up to 500 meters reach on single mode fiber
- Dual MPO- 12 APC
- +3.3V single power supply
- Power Consumption: <16W
- Case operating temperature: 0°C to +70°C
- RoHS 6 Compliant

Applications

- 800G Ethernet
- Data centers and cloud networks

Order Information

Part NO.	Bit Rate	Laser	Distance *1	Fiber Media	DDMI	Connector	Temp *2
LPXWHB31-S50C	850.Gbps	1310nm	500m	SMF	YES	2 X MPO-12 (APC)	0 ~ 70℃

Note:

1. with FEC
2. Case Temperature.

I. Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Storage Temperature	T_S	-40		85	ºC	
Storage Ambient Humidity	H_A	15		85	%	No condensation
Maximum Supply Voltage	V_{CC}	-0.5		3.6	V	
Receiver damage Threshold，per lane		5			dBm	

II. Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	T_C	0	-	+70	°C	
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Power Dissipation	Pd	-	-	16	W	
Supply Current	Icc	-	-	5100	mA	
Pre-FEC Bit Error Ratio	-	-	-	2E-4	-	
Post-FEC Bit Error Ratio	-	-	-	1E-12	-	1
Link Distance with SMF	-	2	-	500	m	2

Note1: FEC provided by host system

Note2: FEC required on host system to support maximum distance

III. Optical Characteristics

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Transmitter						
Signaling Rate per Lane	SR	Gbd	53.125 ± 100 ppm			
Modulation format	-	-	PAM4			
Center wavelength	CW	nm	1304.5	-	1317.5	
Side-mode Suppression ratio (SMSR)	SMSR	dB	30	-	-	
Average Launch Power per Lane	AOP	dBm	-2.9	-	4.0	1
Outer Optical Modulation Amplitude (OMAouter), each lane (min)	OMA	dBm	-0.8	-	4.2	
Launch power in OMAouter minus TDECQ (min)		dBm	-2.2			
Transmitter and Dispersion Eye Closure for PAM4	TDECQ	dB	-	-	3.4	
(TDECQ), each lane						
Average Launch Power of OFF Transmitter, each lane	TOFF	dBm	-	-	-15	

Transmitter reflectance (max)		dB	-	-	-26	
Optical Extinction Ratio	ER	dB	3.5	-	-	
Optical Return Loss Tolerance		dB	-	-	21.4	
Receiver						
Signaling Rate per Lane	SR	Gbd	53.125 ± 100 ppm			
Modulation format	-	-	PAM4			
Wavelength	W	nm	1304.5	-	1317.5	
Average Receive Power, each lane	RXPx	dBm	-5.9	-	4	2
Receive Power (OMAouter), each Lane	RxOMA	dBm	-	-	4.2	3
Receiver Reflectance		dB	-	-	-26	
Stressed Receiver Sensitivity (OMAouter), each Lane		dBm	-	-	-1.9	4
Receiver Sensitivity (OMAouter), each Lane		dBm	-	-	-4.4	

Note1: RMS spectral width is the standard deviation of the spectrum.

Note2: The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.

Note3: Average receive power, each lane (min) is not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

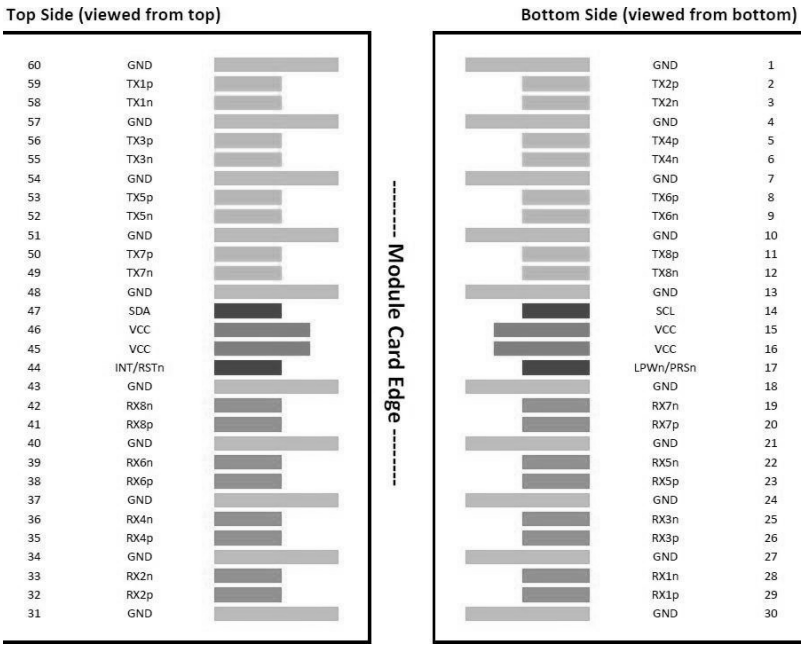
Note4: Receiver sensitivity is informative and is defined for a transmitter with a value of SECQ. Measured with conformance test signal at TP3 for BER=2.4E-4 Pre-FEC.

IV. Electrical Characteristics

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Supply Voltage	V_{CC}	3.135		3.465	V	
Power Dissipation	Pd			16	W	
Transmitter						
Differential pk-pk input Voltage tolerance	-	mV	900	-	-	
Differential termination mismatch	-	%	-	-	10	
Single-ended voltage tolerance range	-	V	-0.4	-	3.3	
DC common mode Voltage	-	mV	-350	-	2850	
Receiver						
AC common-mode output Voltage (RMS)	-	mV	-	-	17.5	
Differential output Voltage	-	mV	-	-	900	
Near-end Eye height, differential	-	mV	70	-	-	

Far-end Eye height, differential	-	mV	30	-	-	
Far end pre-cursor ISI ratio	-	%	-4.5	-	2.5	
Differential Termination Mismatch	-	%	-	-	10	
Transition Time (min, 20% to 80%)	-	ps	9.5	-	-	
DC common mode Voltage	-	mV	-350	-	2850	

V. Pin Diagram



Pin Descriptions

Pin	Name	Logic	Description	Plug Sequence	Notes
1	GND		Ground	1	
2	Tx2p	CML-I	Receiver Data Non-Inverted	3	
3	Tx2n	CML-I	Receiver Data Inverted	3	
4	GND		Ground	1	
5	Tx4p	CML-I	Receiver Data Non-Inverted	3	
6	Tx4n	CML-I	Receiver Data Inverted	3	
7	GND		Ground	1	
8	Tx6p	CML-I	Receiver Data Non-Inverted	3	
9	Tx6n	CML-I	Receiver Data Inverted	3	
10	GND		Ground	1	
11	TX8p	CML-I	Receiver Data Non-Inverted	3	
12	TX8n	CML-I	Receiver Data Inverted	3	
13	GND		Ground	1	
14	SCL	LVCMOS-I/O	2-wire Serial interface clock	3	
15	VCC		+3.3V Power	2	

16	VCC		+3.3V Power	2	
17	LPWn/PRSn	Multi-Level	Low-Power Mode Present	3	1
18	GND		Ground	1	
19	RX7n	CML-O	Receiver Data Inverted	3	
20	RX7p	CML-O	Receiver Data Non-Inverted	3	
21	GND		Ground	1	
22	RX5n	CML-O	Receiver Data Inverted	3	
23	RX5p	CML-O	Receiver Data Non-Inverted	3	
24	GND		Ground	1	
25	RX3n	CML-O	Receiver Data Inverted	3	
26	RX3p	CML-O	Receiver Data Non-Inverted	3	
27	GND		Ground	1	
28	RX1n	CML-O	Receiver Data Inverted	3	
29	RX1p	CML-O	Receiver Data Non-Inverted	3	
30	GND		Ground	1	
31	GND		Ground	1	
32	RX2p	CML-O	Receiver Data Non-Inverted	3	
33	RX2n	CML-O	Receiver Data Inverted	3	
34	GND		Ground	1	
35	RX4p	CML-O	Receiver Data Non-Inverted	3	
36	RX4n	CML-O	Receiver Data Inverted	3	
37	GND		Ground	1	
38	RX6p	CML-O	Receiver Data Non-Inverted	3	
39	RX6n	CML-O	Receiver Data Inverted	3	
40	GND		Ground	1	
41	RX8p	CML-O	Receiver Data Non-Inverted	3	
42	RX8n	CML-O	Receiver Data Inverted	3	
43	GND		Ground	1	
44	INT/RSTn	Multi-Level	Module Interrupt / Reset	3	1
45	VCC		+3.3V Power	2	
46	VCC		+3.3V Power	2	
47	SDA	LVCMOS-I/O	2-wire Serial interface data	3	
48	GND		Ground	1	
49	TX7n	CML-I	Transmitter Data Inverted	3	
50	TX7p	CML-I	Transmitter Data Non-Inverted	3	
51	GND		Ground	1	
52	TX5n	CML-I	Transmitter Data Inverted	3	
53	TX5p	CML-I	Transmitter Data Non-Inverted	3	
54	GND		Ground	1	
55	TX3n	CML-I	Transmitter Data Inverted	3	
56	TX3p	CML-I	Transmitter Data Non-Inverted	3	
57	GND		Ground	1	
58	TX1n	CML-I	Transmitter Data Inverted	3	
59	TX1p	CML-I	Transmitter Data Non-Inverted	3	
60	GND		Ground	1	

Notes:

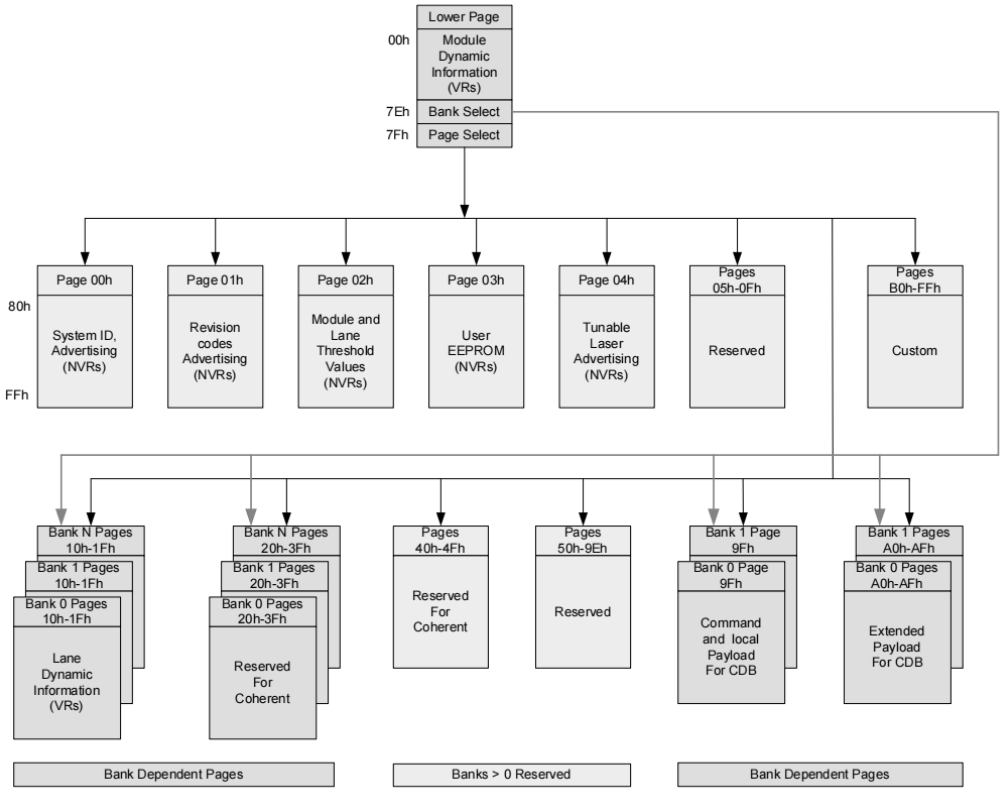
1. Plug Sequence specifies the mating sequence of the host connector and module. The contact sequence is 1,2,3.

2. LPWn/PRSn is a Multi-level signal for low power control from host to module and module presence indication from module to host. It designed according to OSFP Module Specification Section 13.5.3

3. INT/RSTn is a Multi-level signal for interrupt request from module to host and reset control from host to module. It designed according to OSFP Module Specification Section 13.5.2

VI. Memory Map

Compatible with CMIS rev4.0 and upper

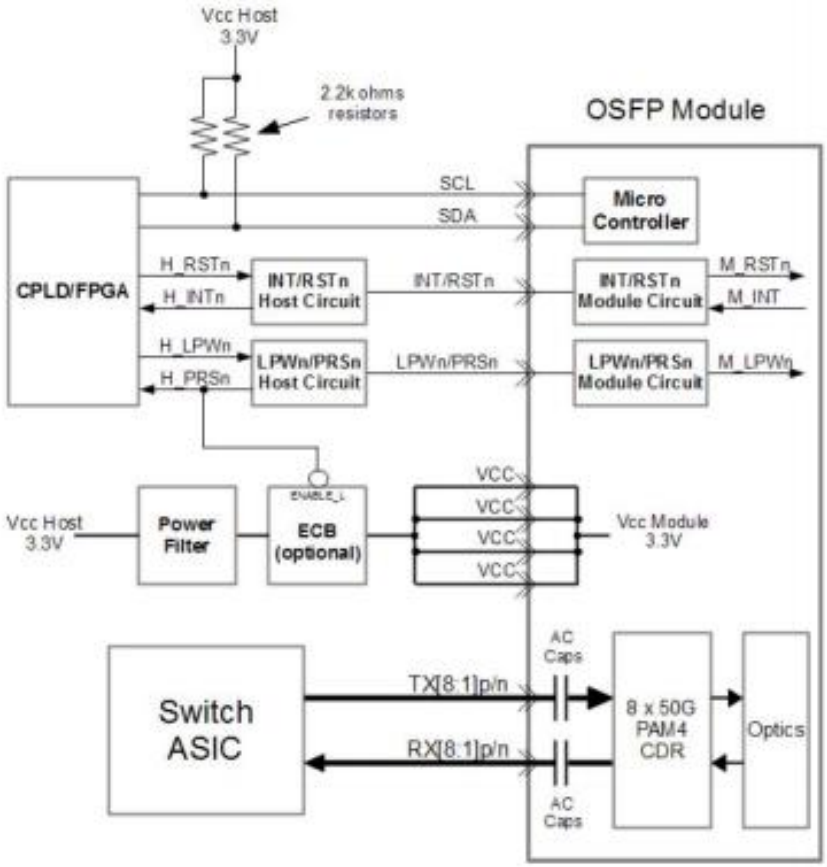


VII. Digital Diagnostic Monitor Accuracy

.Parameter	Symbol	Unit	Min	Max	Notes
Temperature monitor absolute error	DMI_Temp	degC	-3	3	Over operating temperature range
Supply voltage monitor absolute error	DMI _VCC	V	-0.1	0.1	Over full operating range
Channel Bias current monitor	DMI_Ibias_Ch	mA	-10%	10%	
Channel TX power monitor absolute error	DMI_TX_Ch	dB	-3	3	1
Channel RX power monitor absolute error	DMI_RX_Ch	dB	-3	3	1

Note1: Due to measurement accuracy of different multi-mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy

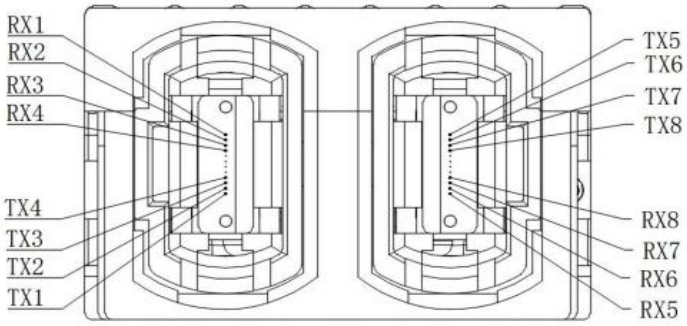
VIII. Recommended Interface



Recommended Interface Circuit

IX. Optical interface arrangement

The optical port is a male MPO connector receptacle,



X. Mechanical Specifications (Unit: mm)