LPWSMB31-S50C

QSFP-DD, 400G DR4,1310nm SMF, 500m

Features

- Supports 4x106Gb/s aggregate bit rate
- 8x26.5625GBd (PAM4) 400GAUI-8 electrical interface
- Hot-pluggable QSFP-DD form factor
- Up to 500m on SMF with FEC
- +3.3V single power supply
- Low power Consumption < 12W
- Optical connector: MPO -12(APC)
- IEE802.3bs 400GBASE-DR4 Specification compliant
- Case operating temperature: 0°C to +70°C
- RoHS compliant

Applications

- 400G Ethernet
- Data centers and cloud networks

Ordering information

Part NO.	Bit Rate	Laser	Distance *1	Fiber Media	DDMI	Connector	Temp *2
LPWSMB31-S50C	425Gbps	1310nm	500	SMF	YES	MPO 1x12 APC	0~70 °C

.

Note: 1.with FEC 2. Case Temperature.

I. Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Ref.
Supply Voltage	Vcc	0	-	3.6	V	
Storage Temperature	Tst	-40		85	°C	
Storage Relative Humidity	H_A	0		85	%	Non-condensation
Receiver damage Threshold	Rin_{dam}	5			dBm	each lane

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II. Recommended Operating Condition

Data Rate Specifications	Symbol	Min.	Typ.	Max.	Unit	Ref.
Operating Case Temperature	TC	0	-	+70	°C	
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	PAM4
Power Dissipation	Pd	-	-	12	W	
Link Distance	-	2	-	500	m	SMF withFEC

III. Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Ref.
Transmitter(per lane)						
Channel data rate	FDC	106.25			Gb/s	
Data rate per lane	F_{SG}	53.125			GBd	PAM4
Center Wavelength	λ_C	1304.5	1311	1317.5	nm	
RMS Spectral Width	σ			0.6	nm	1
Receiver(per lane)						
Damage threshold		5			dBm	2
Average receive power, each lane		–5.9		4.0	dBm	3
Receiver reflectance	Rr			-26	dB	
Receiver sensitivity(OMA outer), each lane	SEN	Max(-3.9,SECQ-5.3)			dBm	4
Stressed receiver sensitivity (OMA outer), each lane	SRS			-1.9	dBm	
Receiver Loss of Signal Indicator Assert Level	LOSA	-15		-7.9	dBm	
Receiver Loss of Signal Indicator De-assert Level	LOSD			-7.5	dBm	
Hysteresis	LOSH	0.5		5	dB	

Notes:

1. RMS spectral width is the standard deviation of the spectrum.

2. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.

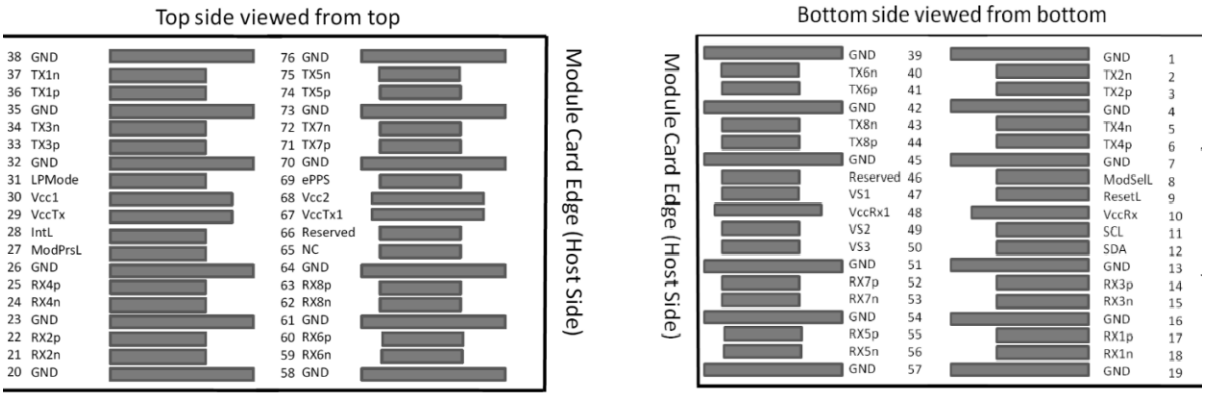
3. Average receive power, each lane (min) is not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

4. Receiver sensitivity is informative and is defined for a transmitter with a value of SECQ. Measured with conformance test signal at TP3 for BER=2.4E-4 Pre-FEC.

IV. Electrical Interface Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Ref.
Supply Voltage	$V_{CC}1$	3.135		3.465	V	
Power Dissipation	Pd			10.5	W	
Transmitter(per Lane)						
Input different impedance	R_{in}	90	100	110	Ω	
Input Logic Level High	-	2		Vcc	V	
Input Logic Level Low	-	0		0.8	V	
Differential data input swing	$V_{in,pp}$			880	mVpp	
Receiver (per Lane)						
Error Bit Rate	BER			2.4E-4		
Output different impedance	R_{out}	90	100	110	Ω	
Output Logic Level High	-	Vcc-0.5		Vcc	V	
Output Logic Level Low	-	0		0.4	V	
Differential data Output swing	$V_{out,pp}$			900	mVpp	

V. Pin Diagram



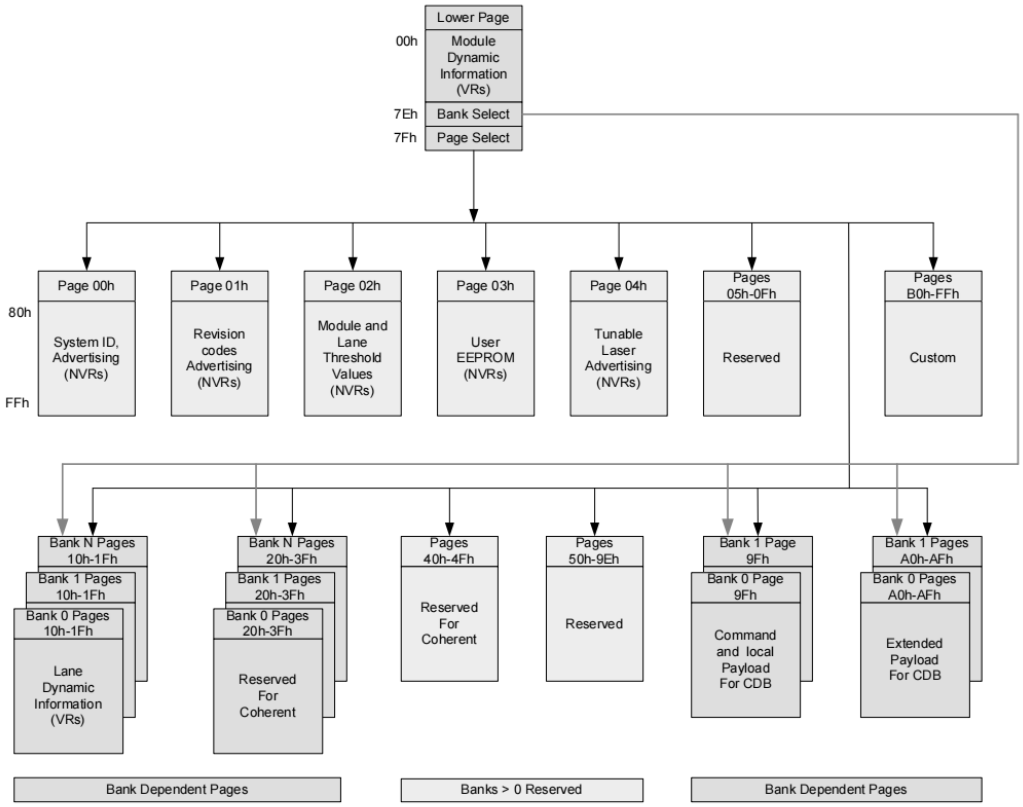
Pin Descriptions:

Pin NO.	Logic	Symbol	Definition	PinNO.	Logic	Symbol	Definition
1		GND	Ground	39		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input	40	CML-I	Tx6n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	41	CML-I	Tx6p	Transmitter Non-inverted Data Input
4		GND	Ground	42		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input	43	CML-I	Tx8n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	44	CML-I	Tx8p	Transmitter Non-inverted Data Input
7		GND	Ground	45		GND	Ground
8	LVTTL-I	ModSelL	Module Select	46		Reserved	
9	LVTTL-I	ResetL	Module Reset	47		VS1	Module Vendor Specific 1
10		VccRx	+3.3V Power Supply Receiver	48		VccRx1	3.3V Power Supply
11	LVCMOS-I/O	SCL	2-wire serial interface clock	49		VS2	Module Vendor Specific 2
12	LVCMOS-I/O	SDA	2-wire serial interface data	50		VS3	Module Vendor Specific 3
13		GND	Ground	51		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output	52	CML-O	Rx7p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output	53	CML-O	Rx7n	Receiver Inverted Data Output
16		GND	Ground	54		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output	55	CML-O	Rx5p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output	56	CML-O	Rx5n	Receiver Inverted Data Output
19		GND	Ground	57		GND	Ground
20		GND	Ground	58		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output	59	CML-O	Rx6n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output	60	CML-O	Rx6p	Receiver Non-inverted Data Output
23		GND	Ground	61		GND	Ground

24	CML-O	Rx4n	Receiver Inverted Data Output	62	CML-O	Rx8n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output	63	CML-O	Rx8p	Receiver Non-inverted Data Output
26		GND	Ground	64		GND	Ground
27	LVTTL-O	ModPrsL	Module Present	65		NC	Not connected
28	LVTTL-O	IntL	Interrupt	66		Reserved	
29		VccTx	+3.3V Power Supply Transmitter	67		VccTx1	3.3V Power Supply
30		Vcc1	+3.3V Power Supply	68		Vcc2	3.3V Power Supply
31	LVTTL-I	InitMode	Initialization mode	69		Reserved	
32		GND	Ground	70		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	71	CML-I	Tx7p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input	72	CML-I	Tx7n	Transmitter Inverted Data Input
35		GND	Ground	73		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	74	CML-I	Tx5p	Transmitter Non-inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input	75	CML-I	Tx5n	Transmitter Inverted Data Input
38		GND	Ground	76		GND	Ground

VI. Memory Map

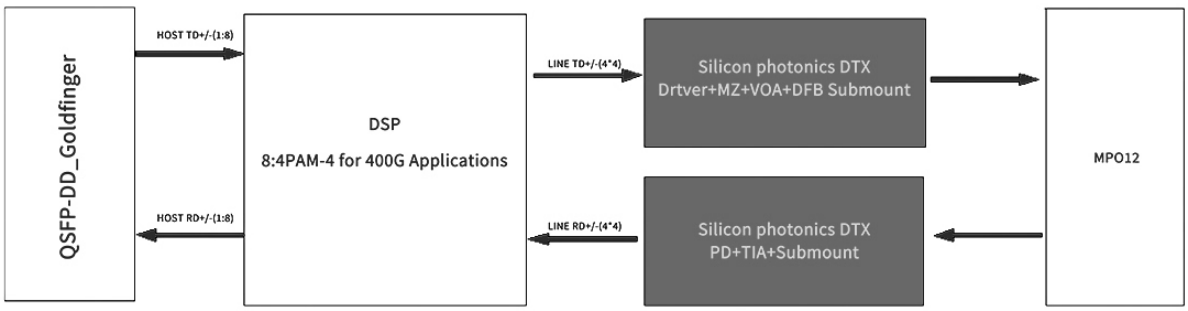
Compatible with CMIS rev4.0 and upper.



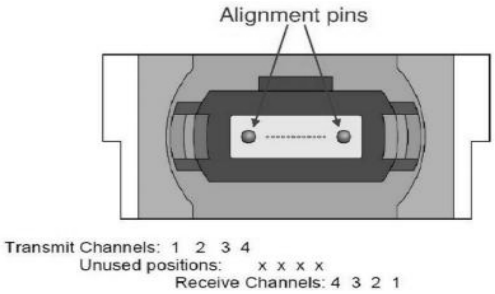
VII. Digital Diagnostic Monitor Accuracy.

Parameter	Accuracy	Unit
Internally Measured Transceiver Temperature	+/-3	℃
Internally Measured Transceiver Supply Voltage	+/-3	%
Measured Tx Bias Current	+/-10	%
Measured Tx Output Power	+/-3	dB
Measured Rx Received Average Optical Power	+/-3	dB

VIII. Functional Block Diagram



IX. Optical interface arrangement



Optical interface arrangement. MPO-12

X. Mechanical Specifications

(Unit: mm)