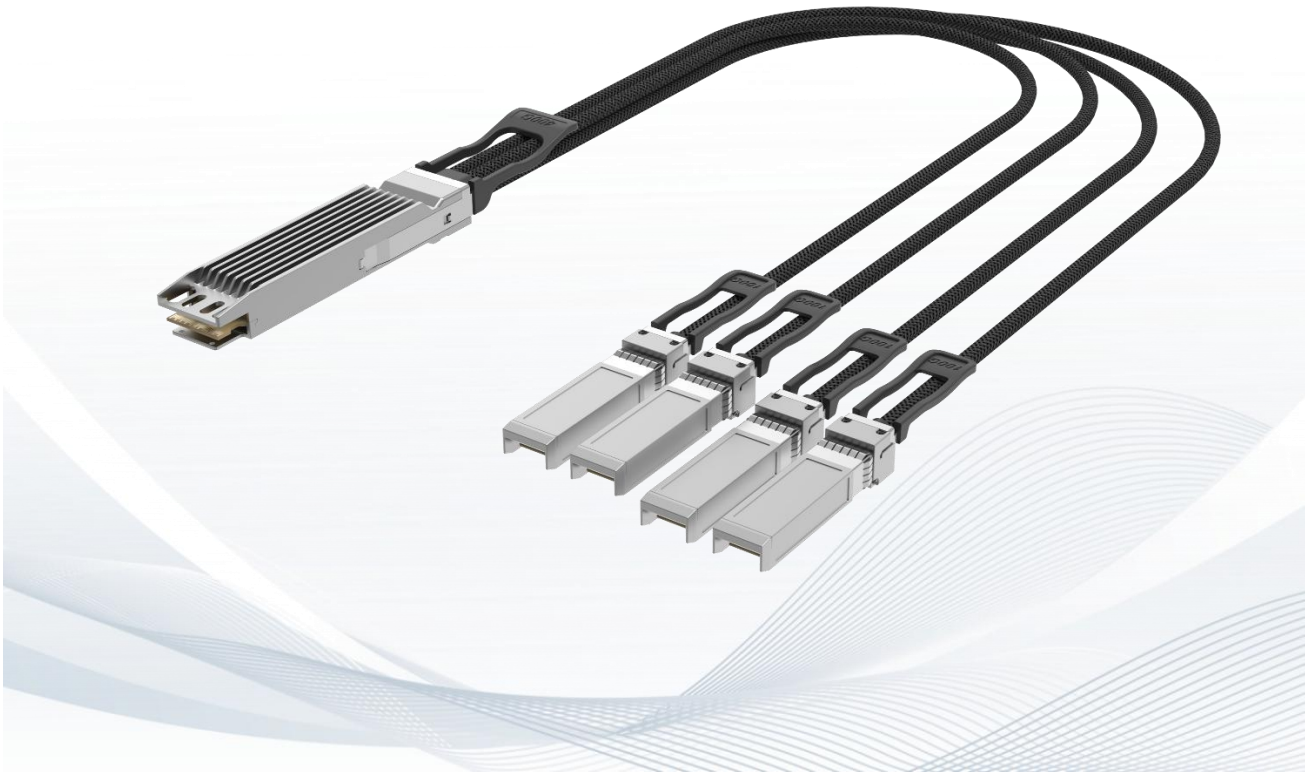
LinkPro™

OSFP 400G to 4X DSFP56 100G Direct Attached Cable Assembly



Application

- Data Center & Networking Equipment
- Servers/Storage Devices
- High Performance Computing (HPC)
- Switches/Routers
- Telecom Central Offices (CO)
- Test And Measurement Equipment

Highlight

- Support 8x56G PAM4
- 400G To 4*(2X50G) Data Rate
- 3.3V Power Supply
- Hot Pluggable
- Excellent SI Performance
- RoHS Compliance
- Simplifies The Patching And Offers A Cost-Effective Way For Short Links

Standards Compliance

- Compliant with OSFP MSA Rev 4.1
- Compliant with DSFP/NGSFP MSA
- Compliant with IEEE 802.3cd
- I2C for EEPROM communication
- Compliant with CMIS 5.0
- SFF-TA-1031,FF-8665, SFF-8661, SFF-8679, SFF-8636

1.0 General Description

This datasheet pertains to the **OSFP 400G to 4*DSFP56 100G Direct Attached Copper Cable Assembly**, meticulously designed for application in the telecommunications and data center sectors. It facilitates bi-directional transmission of 400Gb traffic per cable, accommodating 8 lanes of 56G PAM4. The cable adheres to the standardized OSFP/OSFP-RHS & DSFP28(56) form factor and complies rigorously with Multi-Source Agreement (MSA) specifications.

2.0 Product Specification

2.1 Absolute Maximum Ratings

Parameter	Unit	Min.	Max.	Notes
Supply Voltage	V	-0.3	3.6	
Data Input Voltage	V	-0.3	3.6	
Control Input Voltage	V	-0.3	3.6	
Operating Temperature	°C	0	70	
Storage Temperature	°C	-40	+85	
Relative Humidity (Non-Condensing)	%	5	85	

2.2 Operational Specification

Parameter	Unit	Min	Typical	Max	Notes
Supply Voltage (Vcc)	V	3.135	3.3	3.465	Per End
Power Consumption	W			1.5	Per End
Operating Case Temperature	°C	0		70	
Operating Relative Humidity	%	0		85	
Modulation Format		56G PAM-4			
Bit Rate	Gbps	8x50G to 4*2X50G			

2.3 Electrical Characteristics

Parameter	Unit	Min	Typical	Max	Notes
Characteristic Impedance	ohm	90	100	110	
Time Propagation Delay (Informative)	ns	.....	.....	4.9	

2.4 SI performance

Item	Parameter	Require	Reference
1	ILdd Insertion loss at 13.28 GHz	17.16 dB (Max.)	IEEE 802.3cd Section Section 136.11.2
2	ILdd Insertion loss at 13.28 GHz	8 dB (Min.)	IEEE 802.3cd Section Section 136.11.2
3	ERL Minimum cable assembly	>11 dB*.	IEEE 802.3cd Section Section 136.11.3
4	RLcd Differential-mode to common-mode return loss	0.01GHz – 19GHz Equation (92–28)	IEEE 802.3cd Section 136.11.4
5	ILcd Differential-mode to common-mode insertion loss	0.01GHz – 19GHz Equation (92–29)	IEEE 802.3cd Section 136.11.5
6	RLcc Common-mode to common-mode return loss	0.01GHz – 19GHz Equation (92–30)	IEEE 802.3cd Section Section 136.11.6
7	COM	3dB (Min.)	IEEE 802.3cd Section Section 136.11.7
*Cable assemblies with a com greater than 4 dB are not required to meet minimum ERL			

2.5 Pin Assignments

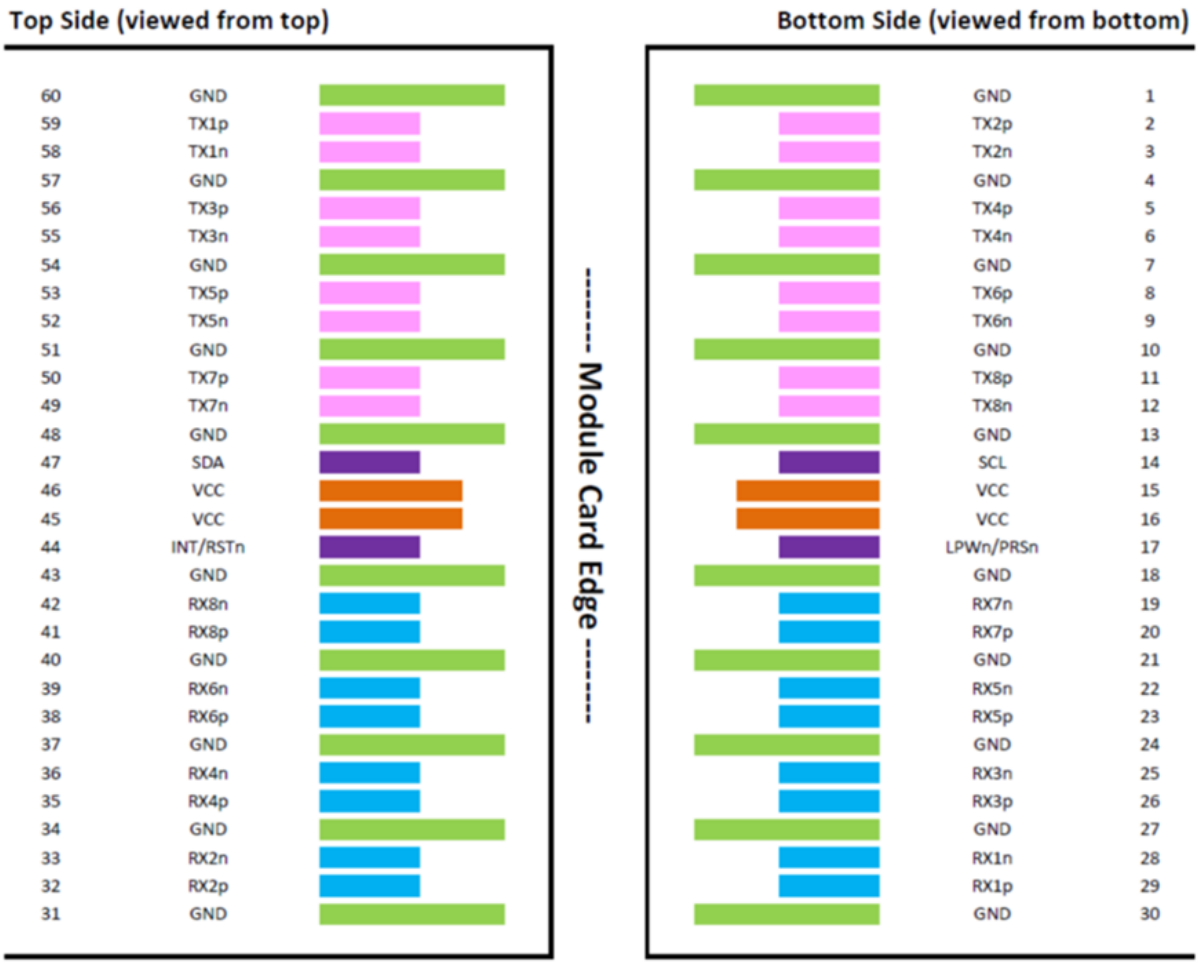


Figure 1 OSFP/OSFP-RHS Module Contact Assignment

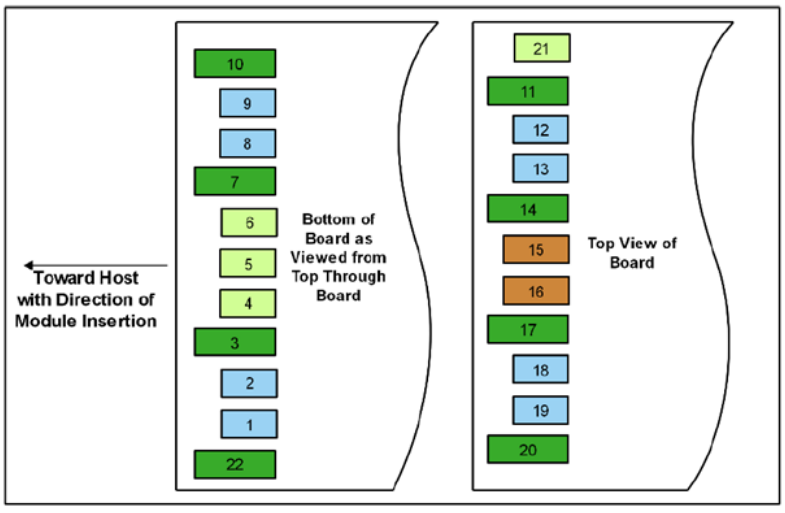


Figure 2 DSFP28(56) Module Contact Assignment

2.6 Pin Description

Table 1 OSFP 400 Module Pin Description

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	
2	CML-I	TX2p	Transmitter Data Non-Inverted	3	
3	CML-I	TX2n	Transmitter Data Inverted	3	
4		GND	Ground	1	
5	CML-I	TX4p	Transmitter Data Non-Inverted	3	
6	CML-I	TX4n	Transmitter Data Inverted	3	
7		GND	Ground	1	
8	CML-I	TX6p	Transmitter Data Non-Inverted	3	
9	CML-I	TX6n	Transmitter Data Inverted	3	
10		GND	Ground	1	
11	CML-I	TX8p	Transmitter Data Non-Inverted	3	
12	CML-I	TX8n	Transmitter Data Inverted	3	
13		GND	Ground	1	
14	LVCMOS-I/O	SCL	2-wire Serial interface clock	3	1
15		VCC	+3.3V Power	2	
16		VCC	+3.3V Power	2	
17	Multi-Level	LPWn/PRSn	Low-Power Mode / Module Present	3	2
18		GND	Ground	1	
19	CML-O	RX7n	Receiver Data Inverted	3	
20	CML-O	RX7p	Receiver Data Non-Inverted	3	
21		GND	Ground	1	
22	CML-O	RX5n	Receiver Data Inverted	3	
23	CML-O	RX5p	Receiver Data Non-Inverted	3	
24		GND	Ground	1	
25	CML-O	RX3n	Receiver Data Inverted	3	
26	CML-O	RX3p	Receiver Data Non-Inverted	3	
27		GND	Ground	1	
28	CML-O	RX1n	Receiver Data Inverted	3	
29	CML-O	RX1p	Receiver Data Non-Inverted	3	
30		GND	Ground	1	
31		GND	Ground	1	
32	CML-O	RX2p	Receiver Data Non-Inverted	3	
33	CML-O	RX2n	Receiver Data Inverted	3	
34		GND	Ground	1	
35	CML-O	RX4p	Receiver Data Non-Inverted	3	
36	CML-O	RX4n	Receiver Data Inverted	3	
37		GND	Ground	1	

38	CML-O	RX6p	Receiver Data Non-Inverted	3	
39	CML-O	RX6n	Receiver Data Inverted	3	
40		GND	Ground	1	
41	CML-O	RX8p	Receiver Data Non-Inverted	3	
42	CML-O	RX8n	Receiver Data Inverted	3	
43		GND	Ground	1	
44	Multi-Level	INT/RSTn	Module Interrupt / Module Reset	3	2
45		VCC	+3.3V Power	2	
46		VCC	+3.3V Power	2	
47	LVCMOS-I/O	SDA	2-wire Serial interface data	3	1
48		GND	Ground	1	
49	CML-I	TX7n	Transmitter Data Inverted	3	
50	CML-I	TX7p	Transmitter Data Non-Inverted	3	
51		GND	Ground	1	
52	CML-I	TX5n	Transmitter Data Inverted	3	
53	CML-I	TX5p	Transmitter Data Non-Inverted	3	
54		GND	Ground	1	
55	CML-I	TX3n	Transmitter Data Inverted	3	
56	CML-I	TX3p	Transmitter Data Non-Inverted	3	
57		GND	Ground	1	
58	CML-I	TX1n	Transmitter Data Inverted	3	
59	CML-I	TX1p	Transmitter Data Non-Inverted	3	
60		GND	Ground	1	
Note 1: Open-Drain with pull- up resistor on Host.					
Note 2: See pin description for required circuit					

Table 2 DSFP28(56) Module Pin Description

Contacts	Logic [1]	Symbol	Power Sequence Order	Name/Description	Note
case		case	See2	Module case	
1	CML-I	TD2-	3rd	Transmitter Inverted Data Input Lane 2	
2	CML-I	TD2+	3rd	Transmitter Non-Inverted Data Input Lane 2	
3		Gnd	1st	Module Ground	5
4	LVTTL-I/O	SDA	3rd	2-wire Serial Interface Data Line	3
5	LVTTL-I/O	SCL	3rd	2-wire Serial Interface Clock	3
6	Multilevel -I/O	LPWn/ PRSn	3rd	Low Power Mode/ Module Present (Mod_Abs)	

7		Gnd	1st	Module Ground	5
8	CML-O	RD2+	3rd	Receiver Non-Inverted Data Output Lane 2	
9	CML-O	RD2-	3rd	Receiver Inverted Data Output Lane 2	
10		Gnd	1st	Module Ground	5
11		Gnd	1st	Module Ground	5
12	CML-O	RD1-	3rd	Receiver Inverted Data Output Lane 1	4
13	CML-O	RD1+	3rd	Receiver Non-Inverted Data Output Lane 1	4
14		Gnd	1st	Module Ground	5
15		Vcc	2nd	Module 3.3 V Supply	
16		Vcc	2nd	Module 3.3 V Supply	
17		Gnd	1st	Module Ground	5
18	CML-I	TD1+	3rd	Transmitter Non-Inverted Data Input Lane 1	4
19	CML-I	TD1-	3rd	Transmitter Inverted Data Input Lane 1	4
20		Gnd	1st	Module Ground	5
21	Multilevel-I/O	INT/RSTn	3rd	Dual Function Module Interrupt and Reset Pin	
22		Gnd	1st	Module Ground	5

Note1:

Labeling as inputs (I) and outputs (O) are from the perspective of the module.

Note2:

The case makes electrical contact to the cage before any of the board edge contacts are made.

Note3:

DSFP 2-wire interface is based on Low Voltage TTL (LVTTL) operating with a module supply of 3.3 V +/-5% and with a host supply range of 2.38 to 3.46 V. The 2-wire interface protocol and electrical specifications are defined in SFF-8431 and compatible with I2C bus specifications.

Note4:

Backward compatible with SFF-8431 SFI interface.

Note5:

The module ground contacts GND recommended to be isolated from the module case by offering flexibility in the host EMI control strategy.

2.7 Cable Wiring

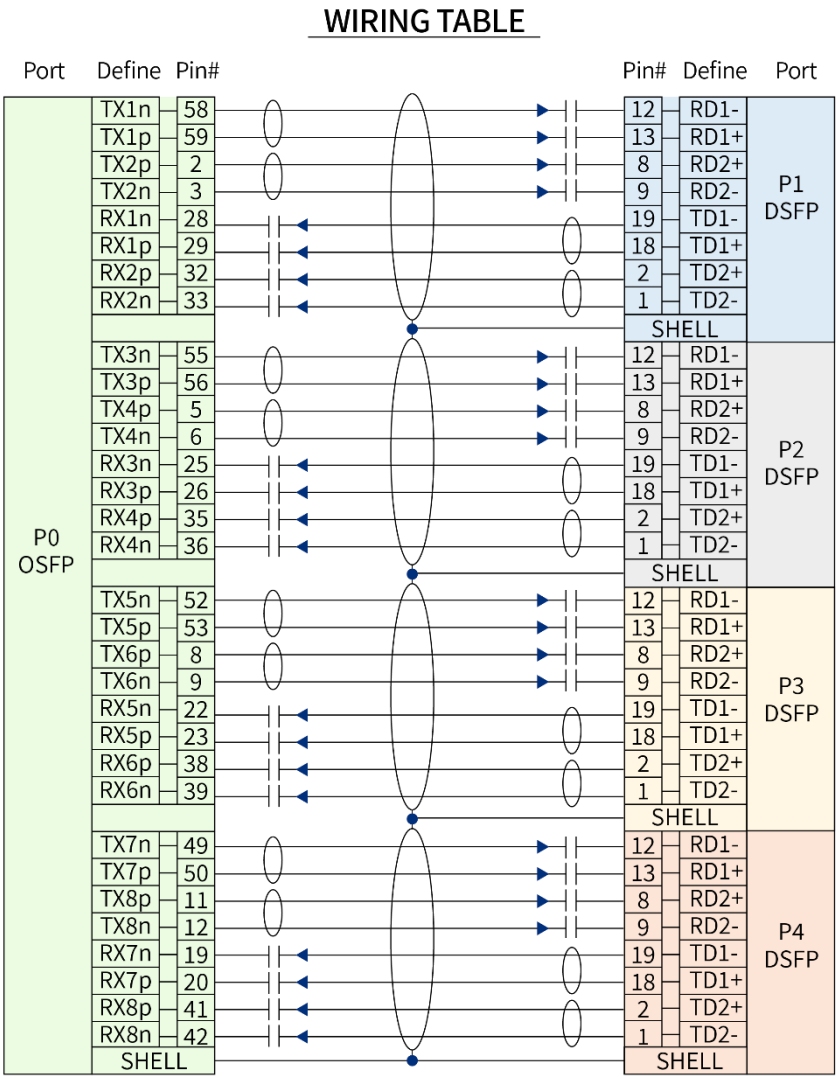


Figure 3 OSFP 400G to 4*DSFP56 Direct Attached cable Wiring

2.8 Memory Map information (CMIS Version)

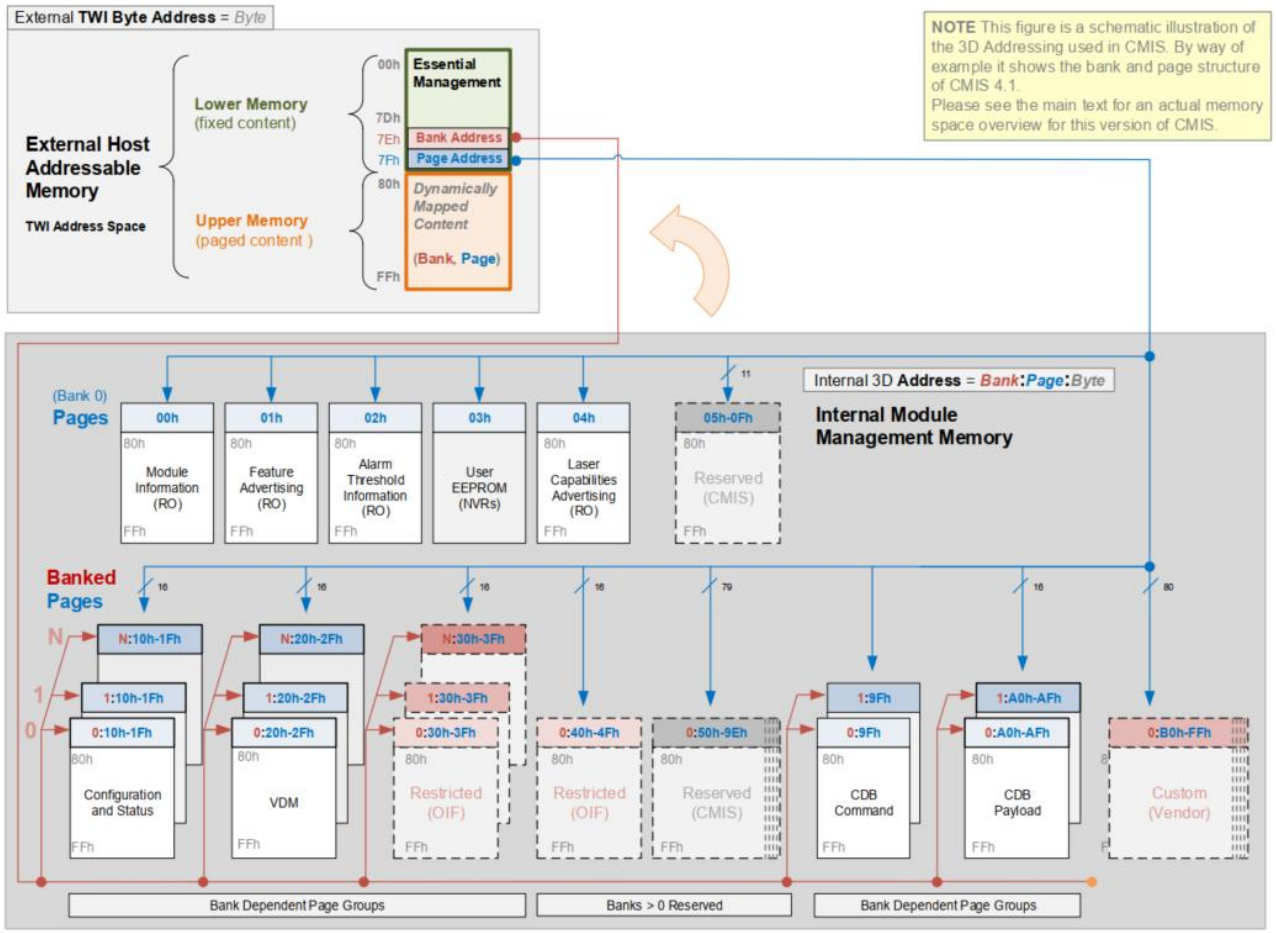


Figure 4 CMIS Module Memory Map (Conceptual View)

Lower Memory Overview

Address	Size	Subject Area	Description
0-3	4	ID and Status Area	Module ID from SFF-8024 list, version number, Type and status
			Flat mem indication, CLEI present indicator, Maximum TWI speed, Current state of Module, Current state of the Interrupt signal
4-7	4	Lane Flag Summary	Flag summary of all lane flags on pages 10h-1Fh
8-13	6	Module-Level Flags	All flags that are not lane or data path specific
14-25	12	Module-Level Monitors	Monitors that are not lane or data path specific
26-3	5	Module Global Controls	Controls applicable to the module as a whole
31-36	6	Module-Level Flag Masks	Masking bits for the Module-Level flags
37-38	2	CDB Status Area	Status of most recent CDB command
39-40	2	Module Firmware Version	Module Firmware Version
41-63	23	Reserved Area	Reserved for future standardization

64-82	19	Custom Area	Vendor or module type specific use
83-84	2	Inactive Firmware Version	Version Number of Inactive Firmware. Values of 00h indicates module supports only a single image.
85-117	33	Application Advertising	Combinations of host and media interfaces that are supported by module data path(s)
118-125	8	Password Entry and Change	
126	1	Bank Select Byte	Bank address of currently visible Page
127	1	Page Select Byte	Page address of currently visible Page

Page 00h Overview

Address	Size (bytes)	Name	Description
128	1	Identifier	Identifier Type of module
129-144	16	Vendor name	Vendor name (ASCII)
145-147	3	Vendor OUI	Vendor IEEE company ID
148-163	16	Vendor PN	Part number provided by vendor (ASCII)
164-165	2	Vendor rev	Revision level for part number provided by vendor (ASCII)
166-181	16	Vendor SN	Vendor Serial Number (ASCII)
182-189	8	Date Code	
190-199	10	CLEI code	Common Language Equipment Identification code
200-201	2	Module power characteristics	
202	1	Cable assembly length	
203	1	Media Connector Type	
204-209	6	Copper Cable Attenuation	
210-211	2	Cable Assembly Lane Information	
212	1	Media Interface Technology	
213-220	8	Reserved	
221	1	Custom	
222	1	Checksum	Includes bytes 128-221
223-255	33	Custom Info NV	

Note: For the above, refer to **Common Management Interface Specification Rev5.0.**

2.9 Memory Map information (SFF-8636 Version)

Table 3 SFF-8636 Memory Map

From	To	Content	No. of bytes	Type
2-Wire Serial Address 1010000x				
Lower Page 00h				
0	2	ID and Status	3	Read-Only
3	21	Interrupt Flags (Clear on read)	19	Read-Only
22	33	Free Side Device Monitors	12	Read-Only
34	81	Channel Monitors	48	Read-Only
82	85	Reserved	4	Read-Only
86	99	Control	14	Read/Write
100	106	Free Side Interrupt Masks	7	Read/Write
107	110	Free Side Device Properties	4	Read-Only
111	112	Assigned to PCI Express	2	Read/Write
113	117	Free Side Device Properties	5	Read-Only
118	118	Reserved	1	Read/Write
119	122	Optional Password Change	4	Write-Only
123	126	Optional Password Entry	4	Write-Only
127	127	Page Select Byte	1	Read/Write
Upper Page 00h				
128	128	Identifier	1	Read-Only
129	191	Base ID Fields	63	Read-Only
192	223	Extended ID	32	Read-Only
224	255	Vendor Specific ID	32	Read-Only

2.10 Mechanical Specifications

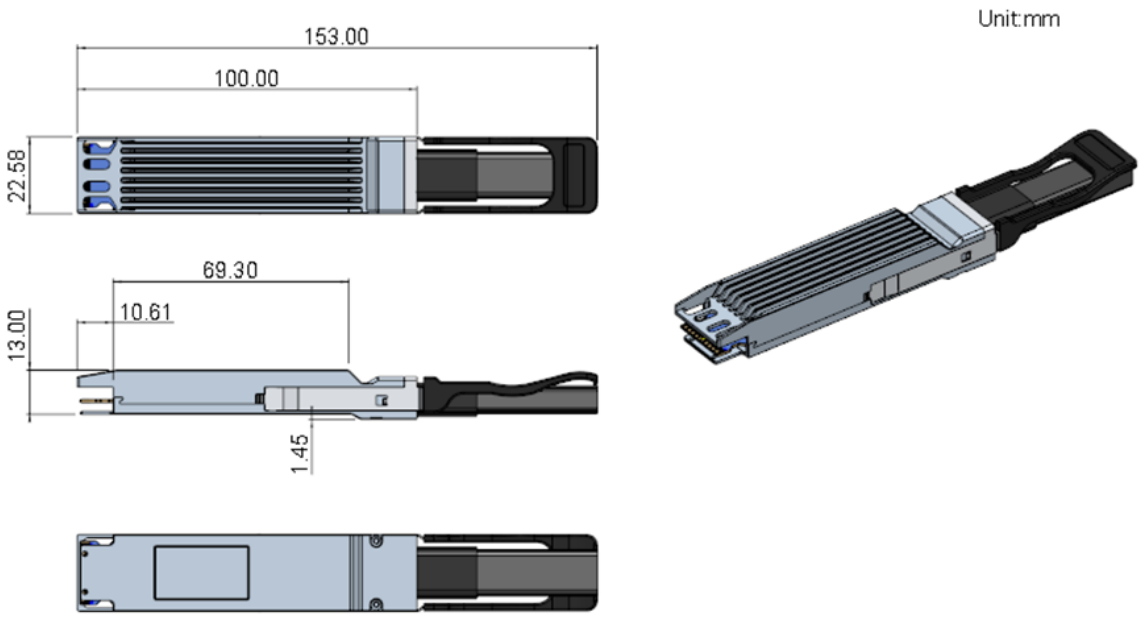


Figure 5 OSFP Form Factor

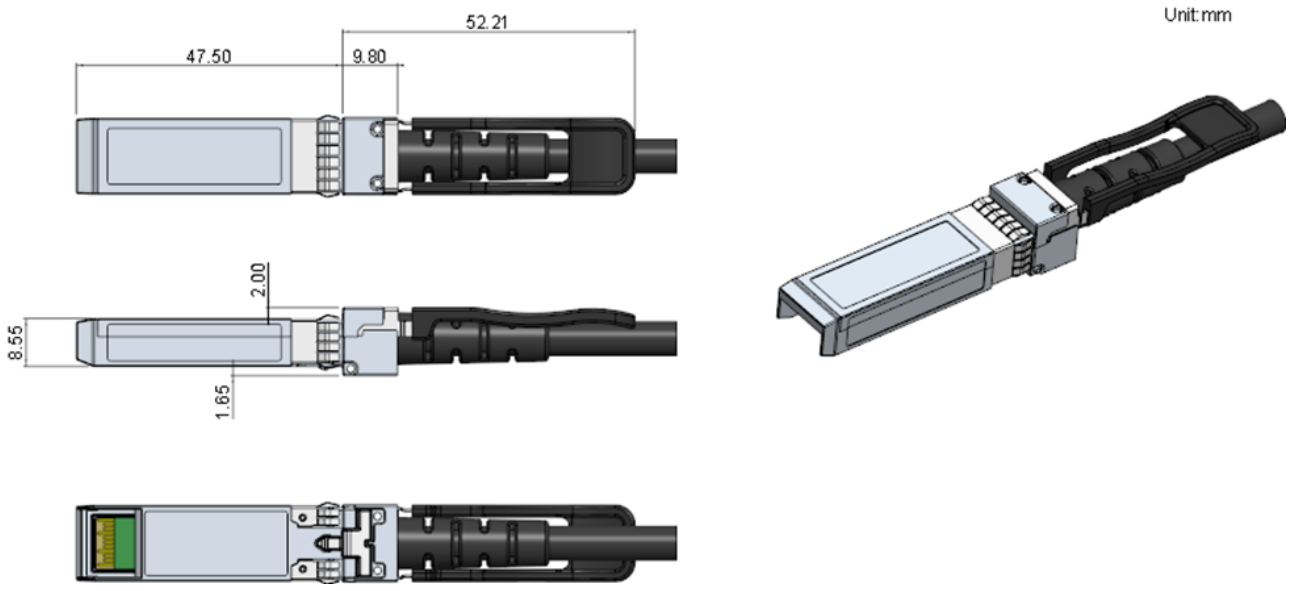
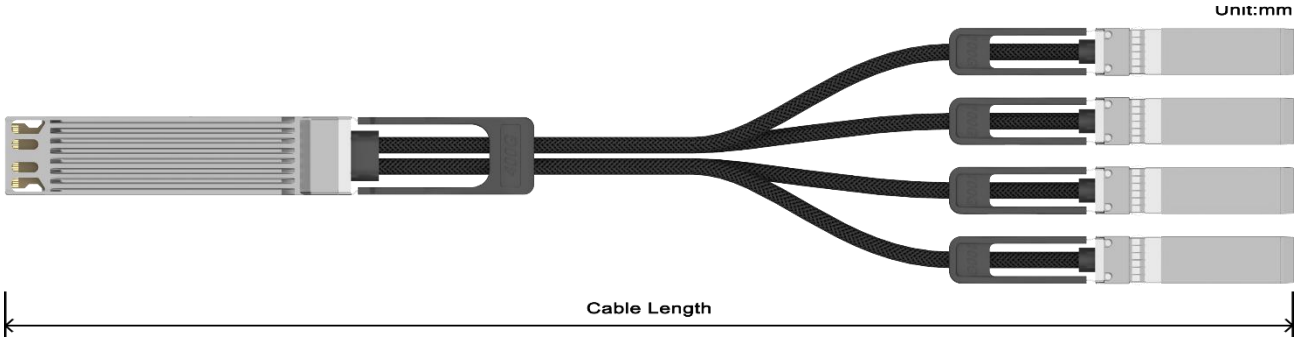


Figure 6 DSFP28(56) Form Factor

3.0 Product Information



Product ID	Product Description	Tolerance	AWG
OSFP-400G-4*DSFP56 100G DAC-3005	OSFP 400G to 4*DSFP56 (2*50G) Direct Attached Copper Cable, 30AWG-0.5M	±20	30
OSFP-400G-4*DSFP56 100G DAC-3010	OSFP 400G to 4*DSFP56 (2*50G) Direct Attached Copper Cable, 30AWG-1.0M	±30	30
OSFP-400G-4*DSFP56 100G DAC-3015	OSFP 400G to 4*DSFP56 (2*50G) Direct Attached Copper Cable, 30AWG-1.5M	±40	30
OSFP-400G-4*DSFP56 100G DAC-3020	OSFP 400G to 4*DSFP56 (2*50G) Direct Attached Copper Cable, 30AWG-2.0M	±40	30
OSFP-400G-4*DSFP56 100G DAC-2820	OSFP 400G to 4*DSFP56 (2*50G) Direct Attached Copper Cable, 28AWG-2.0M	±40	28
OSFP-400G-4*DSFP56 100G DAC-2825	OSFP 400G to 4*DSFP56 (2*50G) Direct Attached Copper Cable, 28AWG-2.5M	±50	28
OSFP-400G-4*DSFP56 100G DAC-2625	OSFP 400G to 4*DSFP56 (2*50G) Direct Attached Copper Cable, 26AWG-2.5M	±50	26
OSFP-400G-4*DSFP56 100G DAC-2630	OSFP 400G to 4*DSFP56 (2*50G) Direct Attached Copper Cable, 26AWG-3.0M	±50	26

Important Notice

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4.0 Revision Record

Rev.	Comments	Author	Date
A01	Initial Release	James Chen	01/16/2024