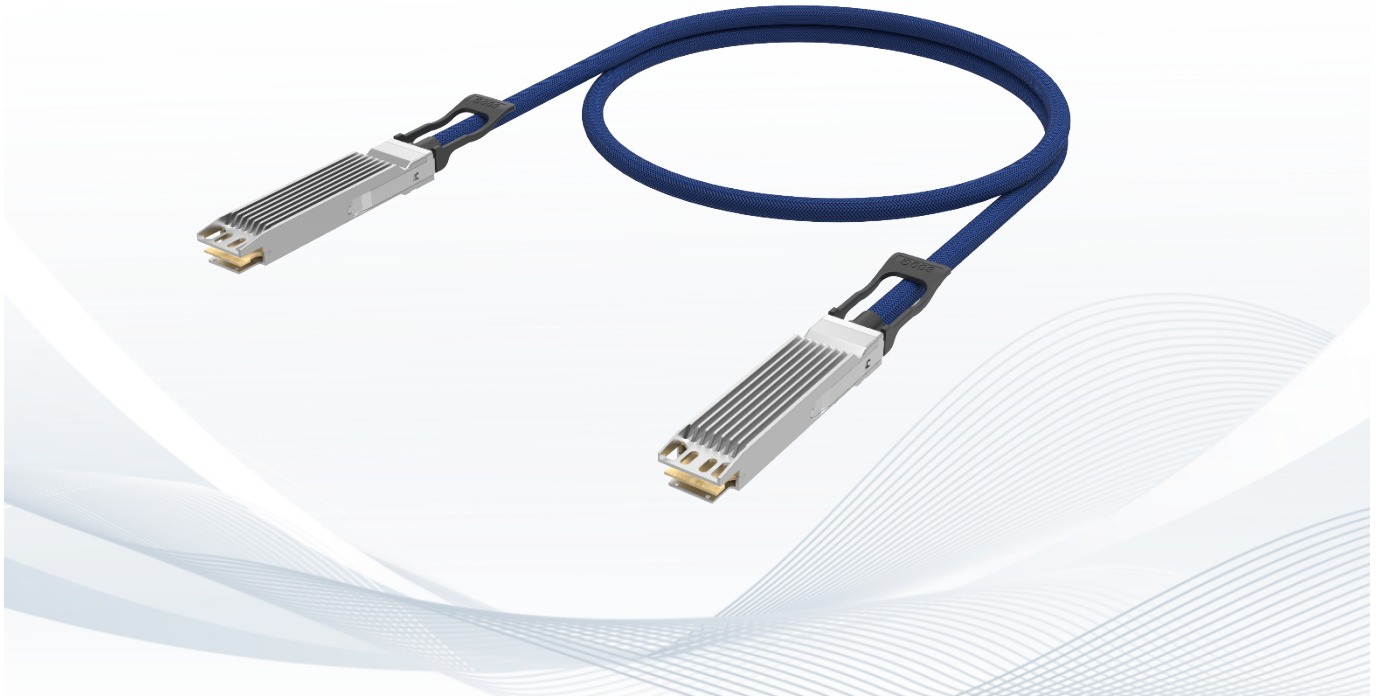




Application

- Data Center & Networking Equipment
- AI Backend Network
- Servers/Storage
- High Performance Computing (HPC)
- Switches/Routers
- Telecom Central Offices (CO)
- Test and Measurement Equipment

Standards Compliance

- Compliant with OSFP MSA
- Compliant with IEEE 802.3ck
- Compliant with IEEE 802.3cd
- I2C for EEPROM Communication
- Compliant with CMIS 5.x

Highlight

- OSFP (8*100G) to OSFP(8*100G) 800G Application
- 3.3V Power Supply
- Hot Pluggable
- Host and line interface support loopbacks and PRBS generator/checker for diagnostic operations
- Performance monitor in features including SNR, eye histogram and more
- Comprehensive test and debug capabilities
- RoHS Compliance
- BER < 10⁻⁸ (Pre FEC)*
- BER < 10⁻¹⁵ (Post FEC)*
 - * Tested with PRBS31Q pattern

1.0 General Description

This datasheet pertains to the **OSFP800-to-OSFP800 800G Active Electrical Cable Assembly** meticulously designed for applications in telecommunications, data centers, and AI backend network sectors. The 800G cable structure consists of an **800G (8x100G-PAM4) OSFP800** connector at both ends, each of which is equipped with a built-in DSP chip. The cable adheres to the standardized **OSFP800** form factor and complies rigorously with Multi-Source Agreement (MSA) specifications.

2.0 Product Specification

2.1 General Product Characteristics

	P1 End	P2 End
Module Form Factor	OSFP800	OSFP800
Full/Half Active Full	Full Active	
Default Data Rate	800G (8*100G-PAM4) to 800G(8*100G-PAM4)	
Numbers of Twin-ax	8 TX and 8 RX (16Pair)	8 TX and 8 RX (16Pair)
Data Rate per Lane	112G-PAM4	112G-PAM4
Cable Construction	Expando over discrete twin-ax and metal braid	
DSP Mode and Data rate (Host to Line Side)	Retimer 8*106.25G to 8*106.25G	Retimer 8*106.25G to 8*106.25G
DSP Brand and Model	Marvell Lynx800	Marvell Lynx800
Management Interface	CMIS 5.x	CMIS 5.x
Nominal Data Rate per Lane	106.25Gbps (PAM4)	106.25Gbps (PAM4)
Pre-FEC Bit Ratio (Test with PRBS31Q Pattern)	<1e-8	<1e-8
Post-FEC Bit Ratio (Test with PRBS31Q Pattern)	<1e-15	<1e-15
Power Consumption per End	11.5W	11.5W
Host Max I2C Interface	400 kbps	
Time to CMIS Ready	100 milliseconds	
Time to Link	15 seconds	
Hot Swappable/Pluggable	Yes	
Maxima Data Rate Capabilities	800G: 112G PAM4 (Data Rate = 106.25 Gbps)	

2.2 Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Storage Temperature	T _{STG}	-40	-	+85	°C	
Supply Voltage	V _{CC}	-0.3	-	3.6	V	
Relative Humidity	RH	10%	-	85%	%	Non-Condensing

2.3 Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Operating Case Temperature	T _{CASE}	0	-	70	°C	
Supply Voltage	V _{CC}	3.135	3.3	3.465	V	
Power Consumption:	P _{DISS}		-		W	
Operating Relative Humidity		0		85	%	

2.4 Electrical Characteristics

Parameter	Min	Typical	Max	Unit	Notes
Characteristic Impedance	90	100	110	ohm	
Time Propagation Delay			4.9	ns	

2.5 . Digital Diagnostic Monitoring Specifications

Parameters	Symbol	Unit	Accuracy	Notes
Temperature Monitor absolute	DMI_TEM	C	±3	Over operating temp
Supply Voltage Monitor absolute	DMI_VCC	%	±5	Full operating range

2.6 Low Speed Electrical Signal Specifications

Parameter	Symbol	Min	Max	Units	Condition
Module output SCL and SDA	VOL	0	0.4	V	IOL(max)=3.0mA for fast mode,20mA for Fast-mode plus
	VOH	V _{CC} -0.5	V _{CC} +0.3	V	
Module input SCL and SDA	VIL	-0.3	V _{CC} *0.3	V	
	VIH	V _{CC} *0.7	V _{CC} +0.5	V	
Capacitance for SCL and SDA I/O pin	Ci		14	pF	

Total bus capacitive load for SCL and SDA	Cb		100	pF	3.0k Ohms Pull up resistor, max
			200	pF	1.6k Ohms Pull up resistor, max
LPMode/TxDis,Reset and ModeSelL	VIL	-0.3	0.8	V	$ I_{in} \leq 125\mu A$ for $V_{in} < V_{cc}$
	VIH	2	$V_{cc} + 0.3$	V	
IntL/RxLOS	VOL	0	0.4	V	IOL=2.0mA
	VOH	$V_{CC} - 0.5$	$V_{CC} + 0.3$	V	10k ohms pull-up to Host V_{cc}
ModPrsL	VOL	0	0.4	%	IOL=2.0mA
	VOH			dB	ModPrsL can implemented as a short-circuit to GND on the module

2.7 Pin Assignments

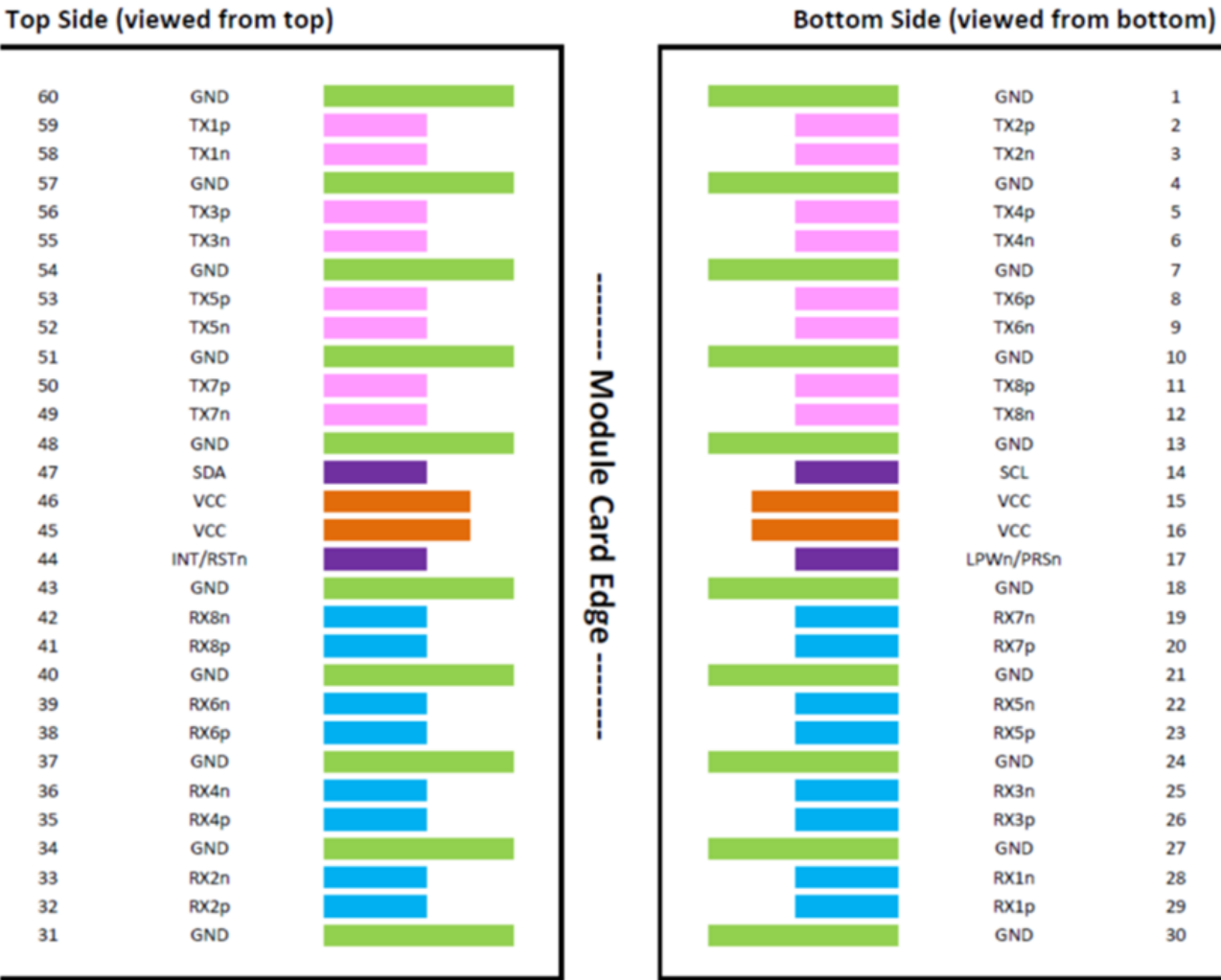


Figure 1 OSFP/OSFP-RHS 800 Module Contact Assignment

Table 1 OSFP800 Module Pin Description

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	
2	CML-I	TX2p	Transmitter Data Non-Inverted	3	
3	CML-I	TX2n	Transmitter Data Inverted	3	
4		GND	Ground	1	
5	CML-I	TX4p	Transmitter Data Non-Inverted	3	
6	CML-I	TX4n	Transmitter Data Inverted	3	
7		GND	Ground	1	
8	CML-I	TX6p	Transmitter Data Non-Inverted	3	
9	CML-I	TX6n	Transmitter Data Inverted	3	
10		GND	Ground	1	
11	CML-I	TX8p	Transmitter Data Non-Inverted	3	
12	CML-I	TX8n	Transmitter Data Inverted	3	
13		GND	Ground	1	
14	LVC MOS-I/O	SCL	2-wire Serial interface clock	3	1
15		VCC	+3.3V Power	2	
16		VCC	+3.3V Power	2	
17	Multi-Level	LPWn/PRSn	Low-Power Mode / Module Present	3	2
18		GND	Ground	1	
19	CML-O	RX7n	Receiver Data Inverted	3	
20	CML-O	RX7p	Receiver Data Non-Inverted	3	
21		GND	Ground	1	
22	CML-O	RX5n	Receiver Data Inverted	3	
23	CML-O	RX5p	Receiver Data Non-Inverted	3	
24		GND	Ground	1	
25	CML-O	RX3n	Receiver Data Inverted	3	
26	CML-O	RX3p	Receiver Data Non-Inverted	3	
27		GND	Ground	1	
28	CML-O	RX1n	Receiver Data Inverted	3	
29	CML-O	RX1p	Receiver Data Non-Inverted	3	
30		GND	Ground	1	
31		GND	Ground	1	
32	CML-O	RX2p	Receiver Data Non-Inverted	3	
33	CML-O	RX2n	Receiver Data Inverted	3	
34		GND	Ground	1	
35	CML-O	RX4p	Receiver Data Non-Inverted	3	
36	CML-O	RX4n	Receiver Data Inverted	3	
37		GND	Ground	1	
38	CML-O	RX6p	Receiver Data Non-Inverted	3	

39	CML-O	RX6n	Receiver Data Inverted	3	
40		GND	Ground	1	
41	CML-O	RX8p	Receiver Data Non-Inverted	3	
42	CML-O	RX8n	Receiver Data Inverted	3	
43		GND	Ground	1	
44	Multi-Level	INT/RSTn	Module Interrupt / Module Reset	3	2
45		VCC	+3.3V Power	2	
46		VCC	+3.3V Power	2	
47	LVC MOS-I/O	SDA	2-wire Serial interface data	3	1
48		GND	Ground	1	
49	CML-I	TX7n	Transmitter Data Inverted	3	
50	CML-I	TX7p	Transmitter Data Non-Inverted	3	
51		GND	Ground	1	
52	CML-I	TX5n	Transmitter Data Inverted	3	
53	CML-I	TX5p	Transmitter Data Non-Inverted	3	
54		GND	Ground	1	
55	CML-I	TX3n	Transmitter Data Inverted	3	
56	CML-I	TX3p	Transmitter Data Non-Inverted	3	
57		GND	Ground	1	
58	CML-I	TX1n	Transmitter Data Inverted	3	
59	CML-I	TX1p	Transmitter Data Non-Inverted	3	
60		GND	Ground	1	

Note 1:

Open-Drain with pull- up resistor on Host.

Note 2:

See pin description for required circuit

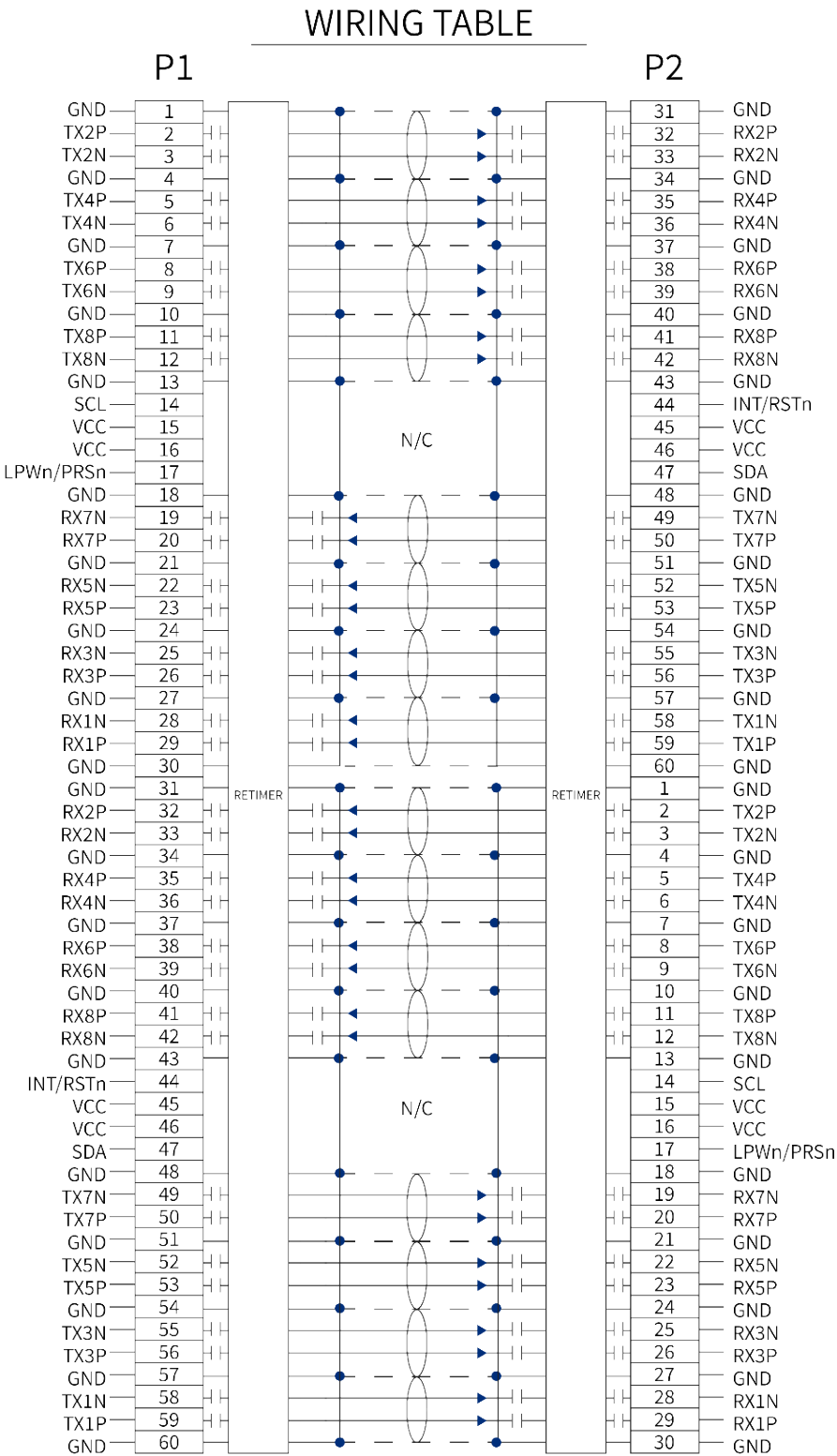


Figure 2 OSFP800 to OSFP800 AEC Wiring

2.10 Memory Map and Control Register (Compatible CMIS 5.x)

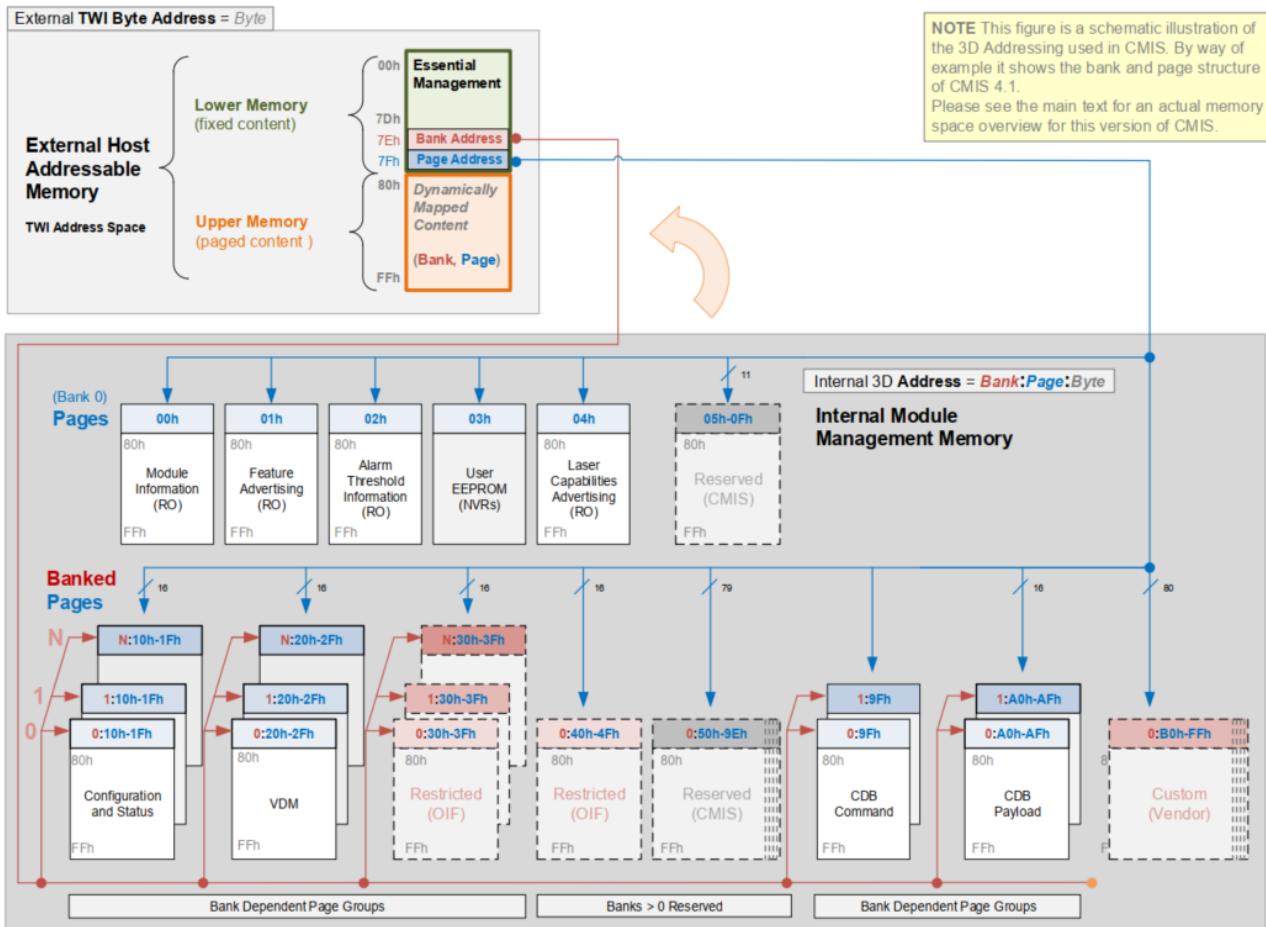


Figure 3 CMIS Module Memory Map (Conceptual View)

2.11 Mechanical Specifications

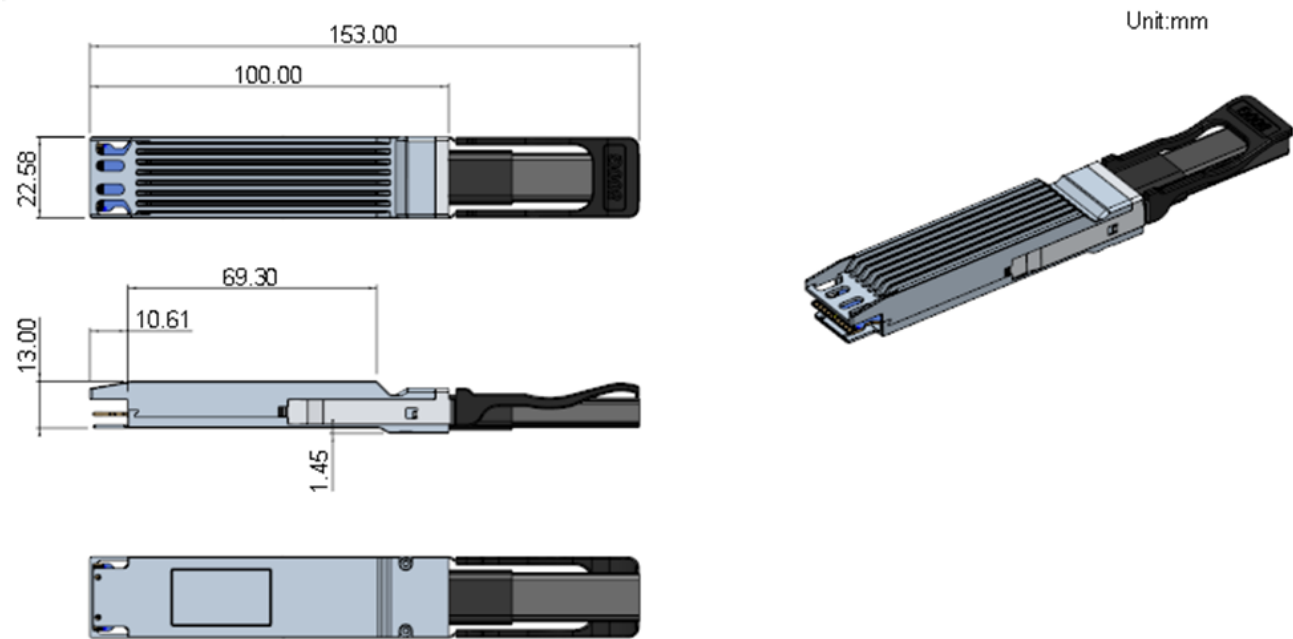
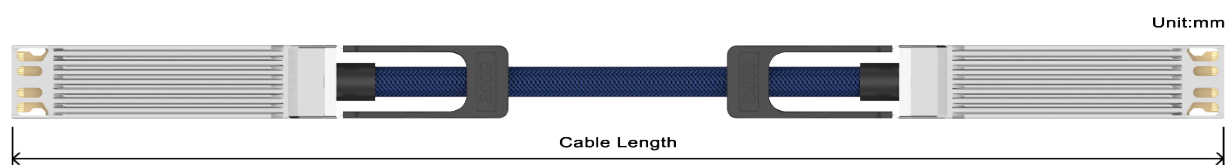


Figure 4 OSFP800 Form Factor

3.0 Product Information



Product ID	Product Description	Tolerance	AWG
OSFP-OSFP 800G-AEC-3210	OSFP to OSFP 800G AEC w/ Marvell Lynx800 DSP ,32AWG-1.0M	±30	32
OSFP-OSFP 800G-AEC-3215	OSFP to OSFP 800G AEC w/ Marvell Lynx800 DSP ,32AWG-1.5M	±40	32
OSFP-OSFP 800G-AEC-3220	OSFP to OSFP 800G AEC w/ Marvell Lynx800 DSP ,32AWG-2.0M	±40	32
OSFP-OSFP 800G-AEC-3225	OSFP to OSFP 800G AEC w/ Marvell Lynx800 DSP ,32AWG-2.5M	±50	30
OSFP-OSFP 800G-AEC-3030	OSFP to OSFP 800G AEC w/ Marvell Lynx800 DSP ,30AWG-3.0M	±50	30
OSFP-OSFP 800G-AEC-3035	OSFP to OSFP 800G AEC w/ Marvell Lynx800 DSP ,30AWG-3.5M	±60	30
OSFP-OSFP 800G-AEC-3040	OSFP to OSFP 800G AEC w/ Marvell Lynx800 DSP ,30AWG-4.0M	±60	30
OSFP-OSFP 800G-AEC-2850	OSFP to OSFP 800G AEC w/ Marvell Lynx800 DSP ,28AWG-5.0M	±70	28
OSFP-OSFP 800G-AEC-2860	OSFP to OSFP 800G AEC w/ Marvell Lynx800 DSP ,28AWG-6.0M	±80	28
OSFP-OSFP 800G-AEC-2870	OSFP to OSFP 800G AEC w/ Marvell Lynx800 DSP ,28AWG-7.0M	±90	28

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4.0Revision Record

Rev.	Comments	Author	Date
A01	Initial Release	James Chen	08/07/2024
A02	Correct spelling typos and add products	James Chen	12/23/2024
A03	Correct typos and change Jacket Color	James Chen	02/15/2025