LinkPro™

QSFP-DD to QSFP-DD-800G Active Electrical Cable Assembly

Application

- Data center & Networking Equipment
- AI Backend Network
- Servers/Storage Devices
- High Performance Computing (HPC)
- Switches/Routers
- Telecom Central Offices (CO)
- Test and Measurement Equipment

Standards Compliance

- Compliant with QSFP-DD MSA
- Compliant with IEEE 802.3ck
- Compliant with IEEE 802.3cd
- I2C for EEPROM Communication
- Compliant with CMIS 5.x

Highlight

- QSFP-DD(8*100G) to QSFP-DD(8*100G) 800G Application
- 3.3V Power Supply
- Hot Pluggable
- Host and line interface support loopbacks and PRBS generator/checker for diagnostic operations
- Performance monitor in features including SNR, eye histogram and more
- Comprehensive test and debug capabilities
- RoHS Compliance
- BER < 10^{-8} (Pre-FEC)*
- BER < 10^{-15} (Post-FEC)*

  * Tested with PRBS31Q pattern

1.0 General Description

This datasheet pertains to the **QSFP-DD800 to QSFP-DD800 800G Active Electrical Cable Assembly,** meticulously designed for applications in telecommunications, data centers, and AI backend network sectors. The 800G cable structure consists of an **800G** (8x100G-PAM4) **QSFP-DD800** connector at both ends, each of which is equipped with a built-in DSP chip. The cable adheres to the standardized **QSFP-DD800** form factor and complies rigorously with Multi-Source Agreement (MSA) specifications.

2.0 Product Specification

2.1 General Product Characteristics

	P1 End	P2 End
Module Form Factor	QSFP-DD800	QSFP-DD800
Full/Half Active Full	Full Active	
Default Data Rate	800G (8*100G-PAM4) to 800G(8*100G-PAM4)	
Numbers of Twin-ax Q'ty Data Rate per Lane	8 TX and 8 RX (16Pair) 112G-PAM4	8 TX and 8 RX (16Pair) 112G-PAM4
Cable Construction	Expando over discrete twin-ax and metal braid	
Module DSP Mode (Host to Line Side)	Retimer 8*106.25G to 8*106.25G	Retimer 8*106.25G to 8*106.25G
DSP Model	Marvell Lynx800	Marvell Lynx800
Management Interface	CMIS 5.x	CMIS 5.x
Nominal Data Rate per Lane	106.25Gbps (PAM4), KP4 FEC must be enabled	106.25Gbps (PAM4), KP4 FEC must be enabled
Pre-FEC Bit Ratio (Test with PRBS31Q Pattern)	<1e-8	<1e-8
Post-FEC Bit Ratio (Test with PRBS31Q Pattern)	<1e-15	<1e-15
Power Consumption per End	11.5W	11.5W
Host Max I2C Interface	400 kbps	
Time to CMIS Ready	100 milliseconds	
Time to Link	15 seconds	
Hot Swappable/Pluggable	Yes	
Maximum Aggregate Data Rate	800G: 112G PAM4 (Data Rate = 106.25 Gbps)	

2.2 Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Storage Temperature	TSTG	-40	-	+85	°C	
Supply Voltage	Vcc	-0.3	-	3.6	V	
Relative Humidity	RH	10%	-	85%	%	Non-Condensing

2.3 Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Operating Case Temperature	TCASE	0	-	70	°C	
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Power Consumption:	PDISS		-		W	
Operating Relative Humidity		0		85	%	

2.4 Electrical Characteristics

Parameter	Min	Typical	Max	**Unit**	Notes
Characteristic Impedance	90	100	110	ohm	
Time Propagation Delay			4.9	ns	

2.5 . Digital Diagnostic Monitoring Specifications

Parameters	Symbol	Unit	Accuracy	**Notes**
Temperature Monitor absolute	DMI_TEM	C	±3	Over operating temp
Supply Voltage Monitor absolute	DMI _VCC	%	±5	Full operating range

2.6 Low Speed Electrical Signal Specifications

Parameter	Symbol	Min	Max	Units	Condition
Module output SCL and SDA	VOL	0	0.4	V	IOL(max)=3.0mA for fast mode,20mA for Fast-mode plus
	VOH	Vcc-0.5	Vcc+0.3	V	
Module input SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	Vcc*0.7	Vcc +0.5	V	
Capacitance for SCL and SDA I/O pin	Ci		14	pF	
Total bus cpacitive	Cb		100	pF	3.0k Ohms Pull up resistor, max

load for SCL and SDA			200	pF	1.6k Ohms Pull up resistor, max
LPMode/TxDis,Reset and ModeSelL	VIL	-0.3	0.8	V	|Iin| </= 125uA for Vin < Vcc
	VIH	2	Vcc + 0.3	V	
IntL/RxLOS	VOL	0	0.4	V	IOL=2.0mA
	VOH	VCC - 0.5	VCC + 0.3	V	10k ohms pull-up to Host Vcc
ModPrsL	VOL	0	0.4	%	IOL=2.0mA
	VOH			dB	ModPrsL can implemented as a short-circuit to GND on the module

2.7 Pin Assignments

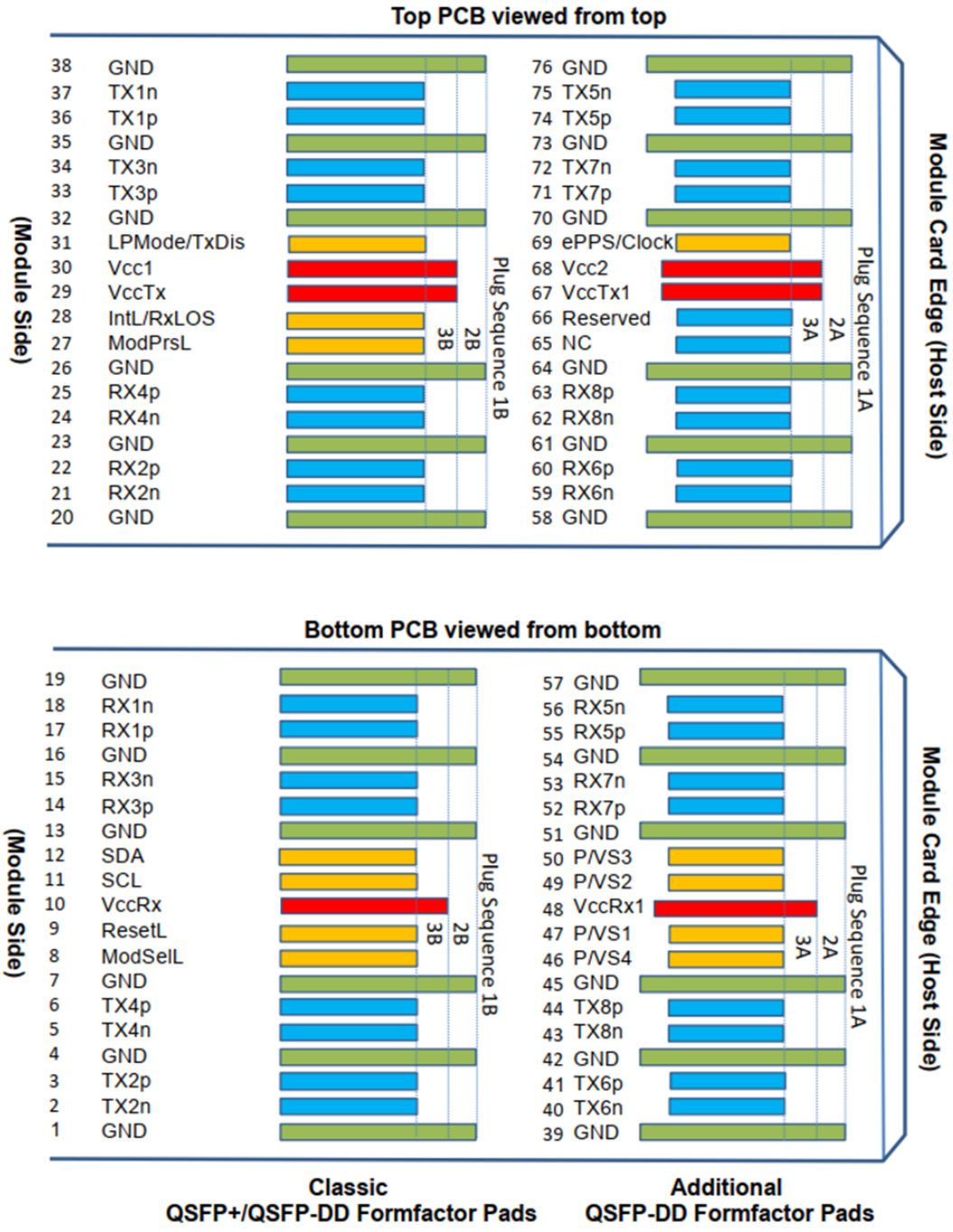


Figure 1 QSFP-DD800 Module Contact Assignment

2.8 Pin Description

Table 1 QSFP-DD800 Module Pin Description

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-1		ModselL	3B	
9	LVTTL-1		ResetL	3B	
10		Vcc Rx	+3.3V Power supply receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface clock	3B	
13		GND	Ground	1B	1
14	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx1n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Present	3B	
28	LVTTL-O	Int/RxLos	Interrupt/optional RxLOS	3B	
29		Vcc Tx	+3.3 V Power supply transmitter	2B	2
30		Vcc1	3.3 V Power supply	2B	2
31	LVTTL-I	LPMode/TxDis	Low Power Mode/optional TX Disable	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46	LVCMOS/CML-I	P/VS4	Programmable/Module Vendor Specific 4	3A	5
47	LVCMOS/CML-I	P/VS1	Programmable/Module Vendor Specific 1	3A	5
48		VccRx1	3.3V Power Supply	2A	2
49	LVCMOS/CML-O	P/VS2	Programmable/Module Vendor Specific 2	3A	5
50	LVCMOS/CML-O	P/VS3	Programmable/Module Vendor Specific 3	3A	5
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVCMOS-I	ePPS/Clock	1PPS PTP clock or reference clock input	3A	6
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note 1:

QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP- DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector GND contact is rated for a steady state current of 500 mA.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector (see MSA specification). For power classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a steady state current of 2000 mA
Note 3: Reserved pad recommended to be terminated with 10 kΩ to ground on the host. Pad 65 (No Connect) Shall be left unconnected within the module, optionally pad 65 may get terminated with 10 kΩ to ground on the host.
Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. Contact sequence A will make, then break contact with additional QSFP- DD pads. Sequence 1A and 1B will then occur simultaneously, followed by 2A and 2B, followed by 3A and 3B
Note 5: Full definitions of the P/VSx signals currently under development. For module designs using programmable/vendor specific inputs P/VS1 and P/VS4 signals it is recommended each to be terminated in the module with 10 kΩ. For host designs using programmable/vendor specific outputs P/VS2 and P/VS3 signals it is recommended each to be terminated on the host with 10 kΩ.
Note 6: For host not implementing ePPS/Clock, it is not necessary to parallel terminate the ePPS/Clock signal to ground on the host. ePPS/Clock already has parallel termination in the module.

2.9 Cable Wiring

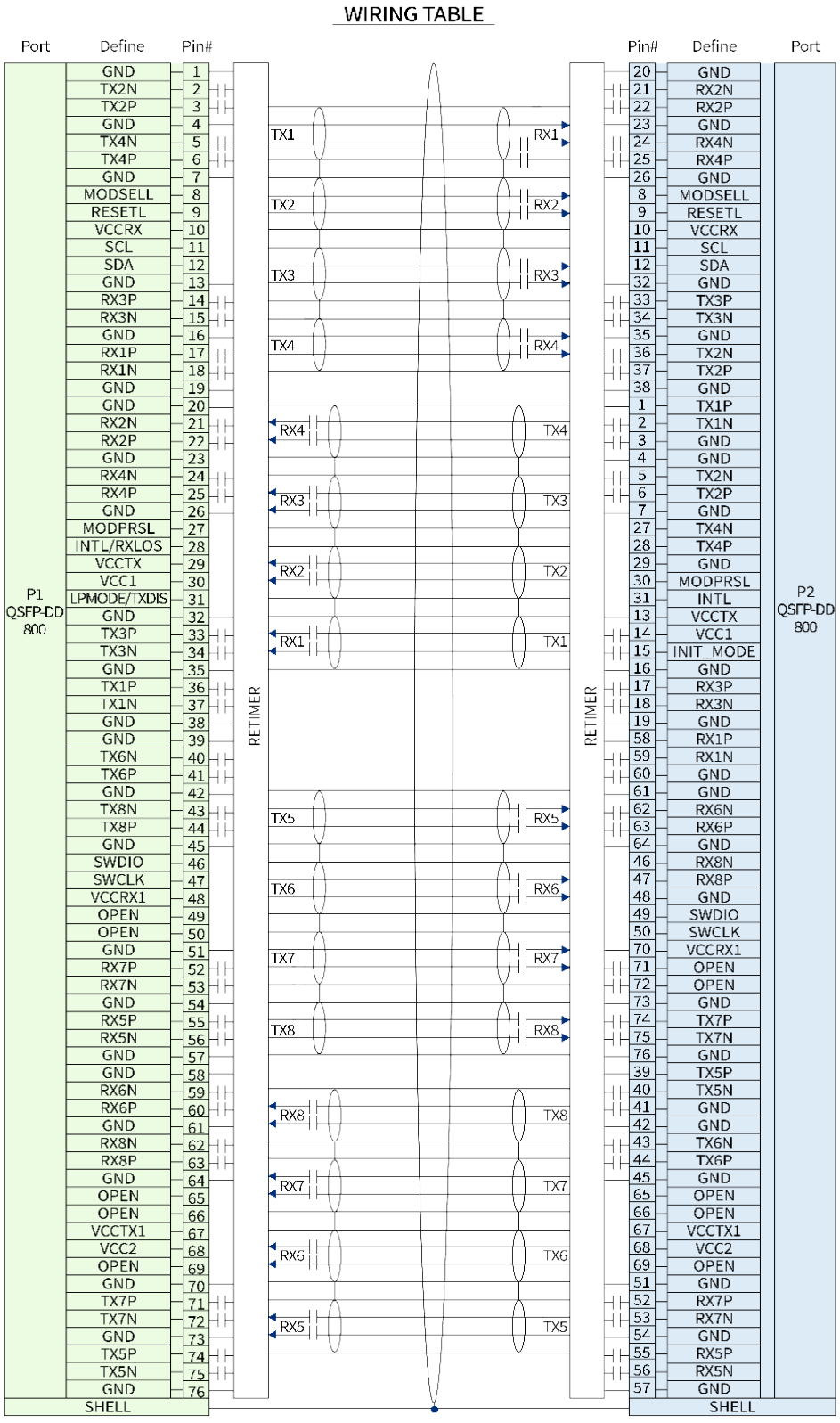


Figure 2 OSFP-DD to QSFP-DD 800G AEC Wiring

2.10 Memory Map and Control Register (Compatible CMIS 5.x)

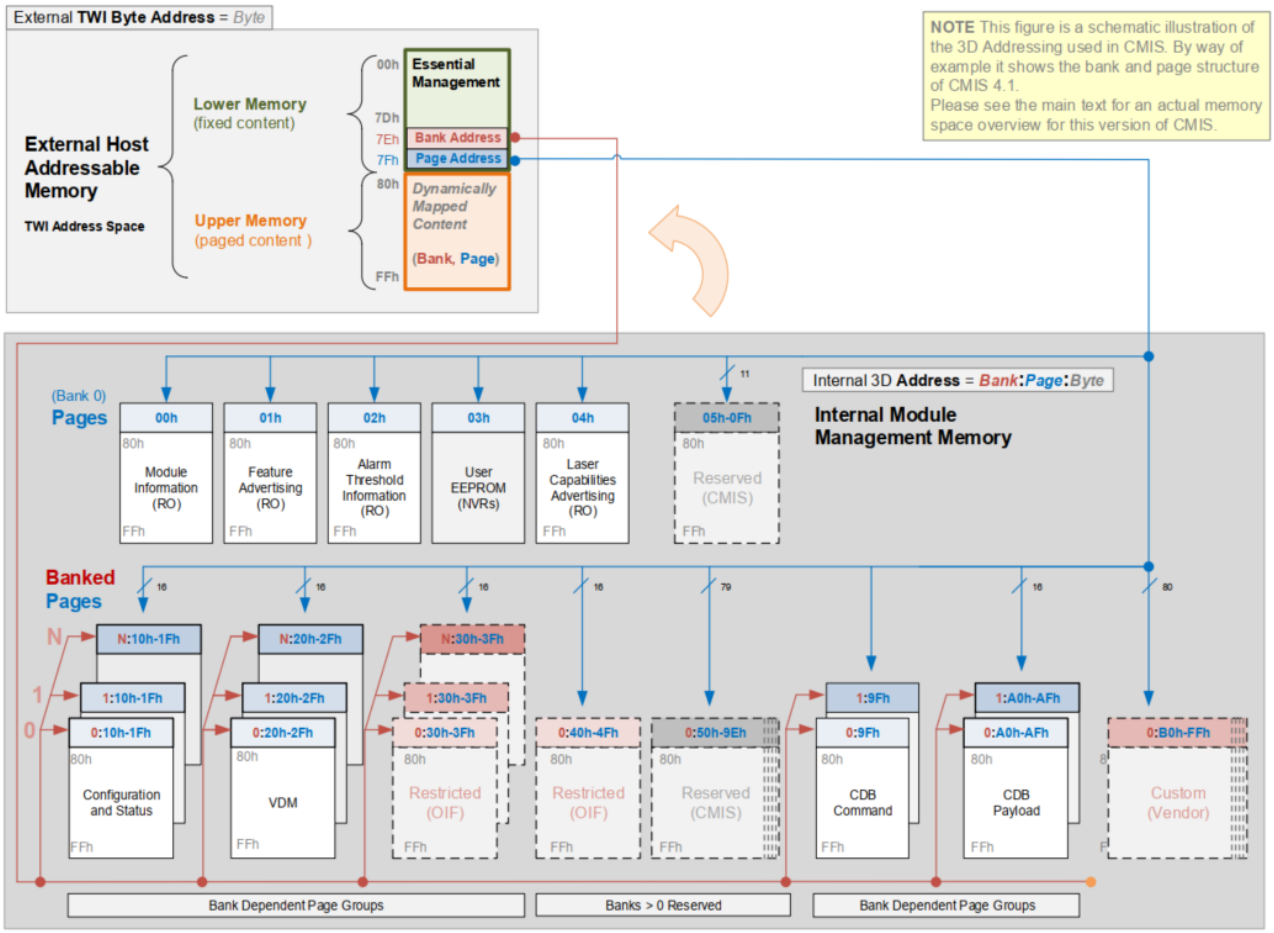


Figure 3 CMIS Module Memory Map (Conceptual View)

2.11 Mechanical Specifications

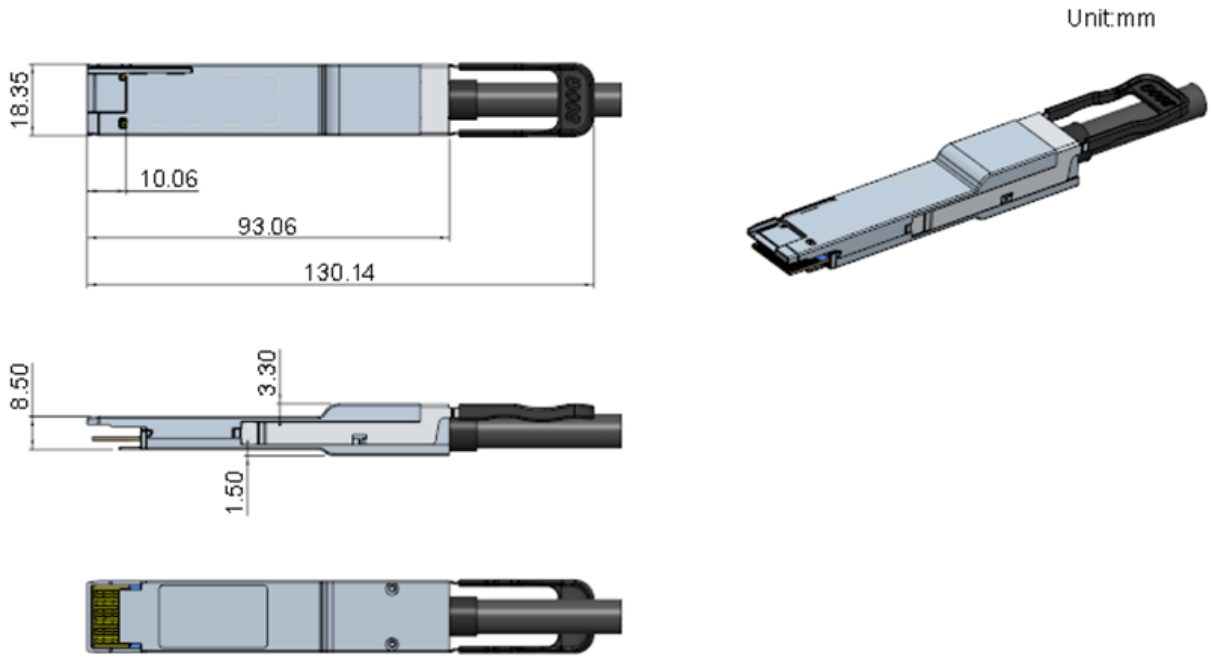
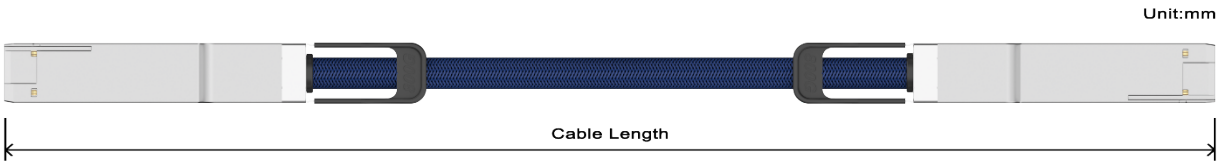


Figure 4 QSFP-DD800 Form Factor

3.0 Product Information



Product ID	Product Description	Tolerance	AWG
QSFP-DD-QSFP-DD 800G-AEC-3210	QSFP-DD to QSFP-DD 800G AEC w/ Marvell Lynx800 DSP ,32AWG-1.0M	±30	32
QSFP-DD-QSFP-DD 800G-AEC-3215	QSFP-DD to QSFP-DD 800G AEC w/ Marvell Lynx800 DSP ,32AWG-1.5M	±40	32
QSFP-DD-QSFP-DD 800G-AEC-3220	QSFP-DD to QSFP-DD 800G AEC w/ Marvell Lynx800 DSP ,32AWG-2.0M	±40	32
QSFP-DD-QSFP-DD 800G-AEC-3225	QSFP-DD to QSFP-DD 800G AEC w/ Marvell Lynx800 DSP ,32AWG-2.5M	±50	30
QSFP-DD-QSFP-DD 800G-AEC-3030	QSFP-DD to QSFP-DD 800G AEC w/ Marvell Lynx800 DSP ,30AWG-3.0M	±50	30
QSFP-DD-QSFP-DD 800G-AEC-3035	QSFP-DD to QSFP-DD 800G AEC w/ Marvell Lynx800 DSP ,30AWG-3.5M	±60	30
QSFP-DD-QSFP-DD 800G-AEC-3040	QSFP-DD to QSFP-DD 800G AEC w/ Marvell Lynx800 DSP ,30AWG-4.0M	±60	30
QSFP-DD-QSFP-DD 800G-AEC-2850	QSFP-DD to QSFP-DD 800G AEC w/ Marvell Lynx800 DSP ,28AWG-5.0M	±70	28
QSFP-DD-QSFP-DD 800G-AEC-2860	QSFP-DD to QSFP-DD 800G AEC w/ Marvell Lynx800 DSP ,28AWG-6.0M	±80	28
QSFP-DD-QSFP-DD 800G-AEC-2870	QSFP-DD to QSFP-DD 800G AEC w/ Marvell Lynx800 DSP ,28AWG-7.0M	±90	28

Important Notice

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4.0Revision Record

Rev.	Comments	Author	Date
A01	Initial Release	James Chen	08/07/2024
A02	Correct spell typo and add Products	James Chen	12/23/204
A03	Correct typos and Chang Jacket Color	James Chen	01/15/204