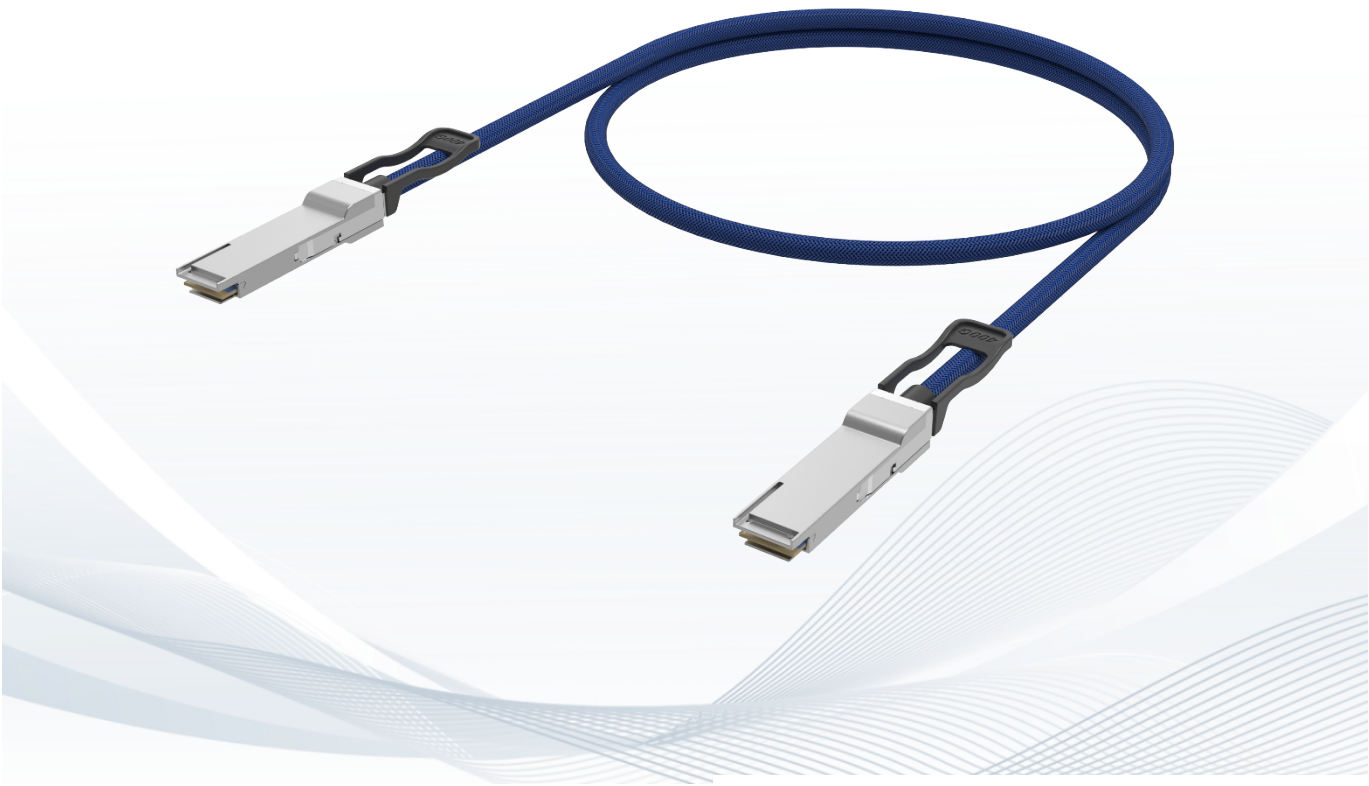
LinkPro™

QSFP112 to QSFP112 400G Active Electrical Cable Assembly



Application

- Data center & Networking Equipment
- AI Backend Network
- Servers/Storage Devices
- High Performance Computing (HPC)
- Switches/Routers
- Telecom Central Offices (CO)
- Test and Measurement Equipment

Standards Compliance

- Compliant with QSFP112 MSA
- Compliant with SFF-1027 MSA
- Compliant with IEEE 802.3ck
- Compliant with IEEE 802.3cd
- I2C for EEPROM Communication
- Compliant with CMIS 5.x

Highlight

- QSFP112(4*100G) to QSFP112(4*100G) 400G Application
- 3.3V Power Supply
- Hot Pluggable
- Host and line interface support loopbacks and PRBS generator/checker for diagnostic operations
- Performance monitor in features including SNR, eye histogram and more
- Comprehensive test and debug capabilities
- RoHS Compliance
- BER < 10^{-8} (Pre-FEC)*
- BER < 10^{-15} (Post-FEC)*

  * Tested with PRBS31Q pattern

1.0 General Description

This datasheet pertains to the **QSFP112-to-QSFP112 400G Active Electrical Cable Assembly** meticulously designed for applications in telecommunications, data centers, and AI backend network sectors. The 400G cable structure consists of a **400G** (4x100G-PAM4) **QSFP112** connector at both ends, each of which is equipped with a built-in DSP chip. The cable adheres to the standardized **QSFP112** form factor and complies rigorously with Multi-Source Agreement (MSA) specifications.

2.0 Product Specification

2.1 General Product Characteristics

	P1 End	P2 End
Module Form Factor	QSFP112	QSFP112
Full/Half Active Full	Full Active	
Default Data Rate	400G (4*100G-PAM4) to 400G(4*100G-PAM4)	
Numbers of Twin-ax Data Rate per Lane	4 TX and 4 RX (8Pair) 112G-PAM4	4 TX and 4 RX (8Pair) 112G-PAM4
Cable Construction	Expando over discrete twin-ax and metal braid	
Module DSP Mode (Host to Line Side)	Retimer 4*106.25G to 4*106.25G	Retimer 4*106.25G to 4*106.25G
DSP Model	Marvell Lynx400	Marvell Lynx400
Management Interface	CMIS 5.x	CMIS 5.x
Nominal Data Rate per Lane	106.25Gbps (PAM4), KP4 FEC must be enabled	106.25Gbps (PAM4), KP4 FEC must be enabled
Pre-FEC Bit Ratio (Test with PRBS31Q Pattern)	<1e-8	<1e-8
Post-FEC Bit Ratio (Test with PRBS31Q Pattern)	<1e-15	<1e-15
Power Consumption per End	8W	8W
Host Max I2C Interface	400 kbps	
Time to CMIS Ready	100 milliseconds	
Time to Link	15 seconds	
Hot Swappable/Pluggable	Yes	
Maxima Data Rate Capabilities	400G: 112G-PAM4(Data Rate = 106.25 Gbps)	

2.2 Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Storage Temperature	TSTG	-40	-	+85	°C	
Supply Voltage	VCC	-0.3	-	3.6	V	
Relative Humidity	RH	10%	-	85%	%	Non-Condensing

2.3 Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Operating Case Temperature	TCASE	0	-	70	°C	
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Power Consumption:	PDISS		-		W	
Operating Relative Humidity		0		85	%	

2.4 Electrical Characteristics

Parameter	Min	Typical	Max	**Unit**	Notes
Characteristic Impedance	90	100	110	ohm	
Time Propagation Delay			4.9	ns	

2.5 . Digital Diagnostic Monitoring Specifications

Parameters	Symbol	Unit	Accuracy	**Notes**
Temperature Monitor absolute	DMI_TEM	C	±3	Over operating temp
Supply Voltage Monitor absolute	DMI _VCC	%	±5	Full operating range

2.6 Low Speed Electrical Signal Specifications

Parameter	Symbol	Min	Max	Units	Condition
Module output SCL and SDA	VOL	0	0.4	V	IOL(max)=3.0mA for fast mode,20mA for Fast-mode plus
	VOH	Vcc-0.5	Vcc+0.3	V	
Module input SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	Vcc*0.7	Vcc +0.5	V	
Capacitance for SCL and SDA I/O pin	Ci		14	pF	
Total bus cpacitive	Cb		100	pF	3.0k Ohms Pull up resistor, max

load for SCL and SDA			200	pF	1.6k Ohms Pull up resistor, max
LPMode/TxDis,Reset and ModeSeIL	VIL	-0.3	0.8	V	|Iin| </= 125uA for Vin < Vcc
	VIH	2	Vcc + 0.3	V	
IntL/RxLOS	VOL	0	0.4	V	IOL=2.0mA
	VOH	VCC - 0.5	VCC + 0.3	V	10k ohms pull-up to Host Vcc
ModPrsL	VOL	0	0.4	%	IOL=2.0mA
	VOH			dB	ModPrsL can implemented as a short-circuit to GND on the module

2.7 Pin Assignments

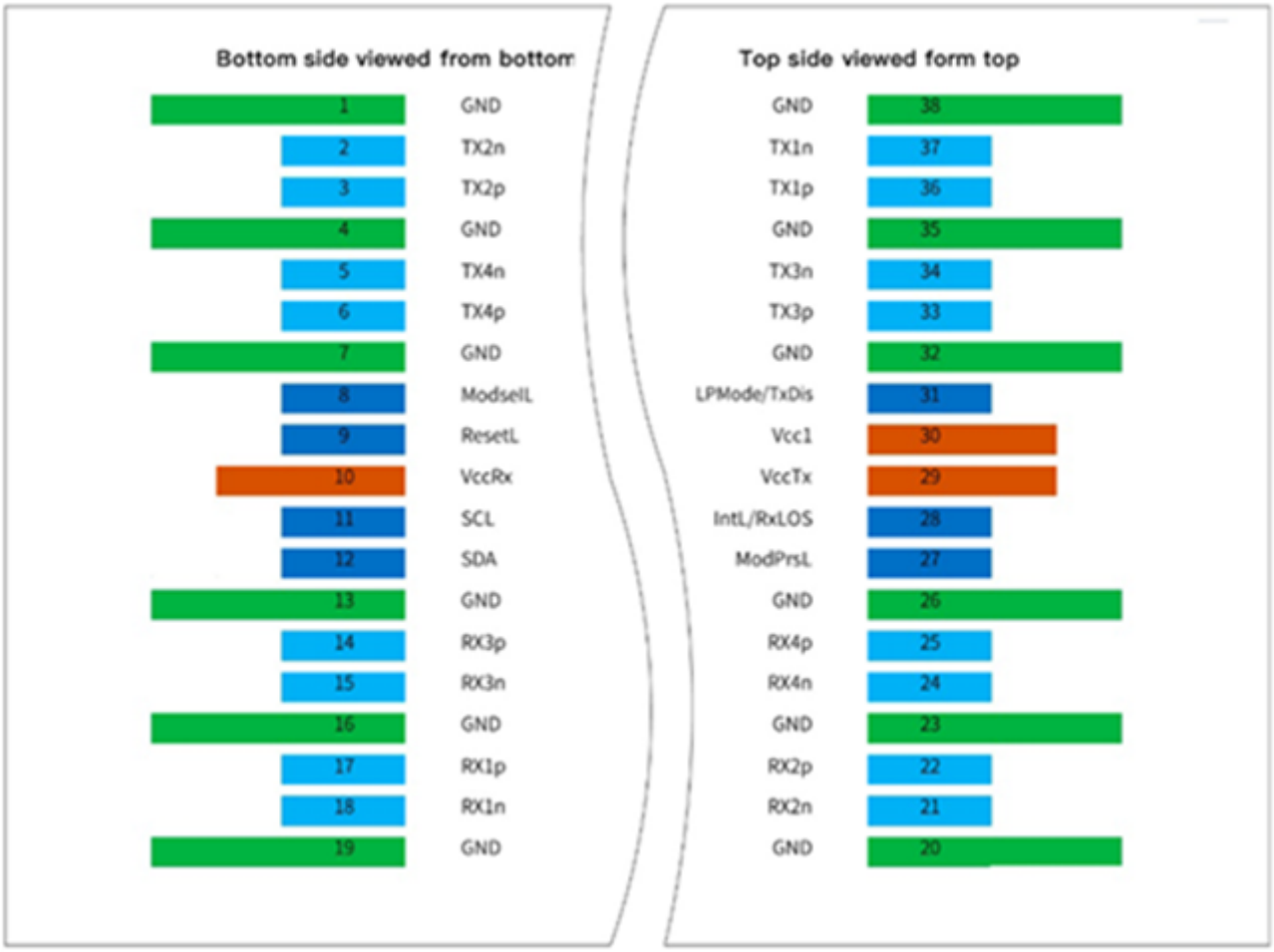


Figure 1 QSFP112 Module Contact Assignment

2.8 Pin Description

Table 1 QSFP112 Module Pin Description

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-1	ModselL	Module Select	3	
9	LVTTL-1	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power supply receiver	2	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface clock	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Present	3	
28	LVTTL-O	Int/RxLos	Interrupt/optional RxLOS	3	
29		Vcc Tx	+3.3 V Power supply transmitter	2	2
30		Vcc1	3.3 V Power supply	2	2
31	LVTTL-I	LPMode/TxDis	Low Power Mode/optional TX Disable	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Note 1: GND is the symbol for signal and supply (power) common for the QSFP112 module. All are common within the QSFP112 module, and all voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane
Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. The connector pins are each rated for a maximum current of 1.5A (max. current of 2.0 A is required for high module power of 15-20W).

2.9 Cable Wiring

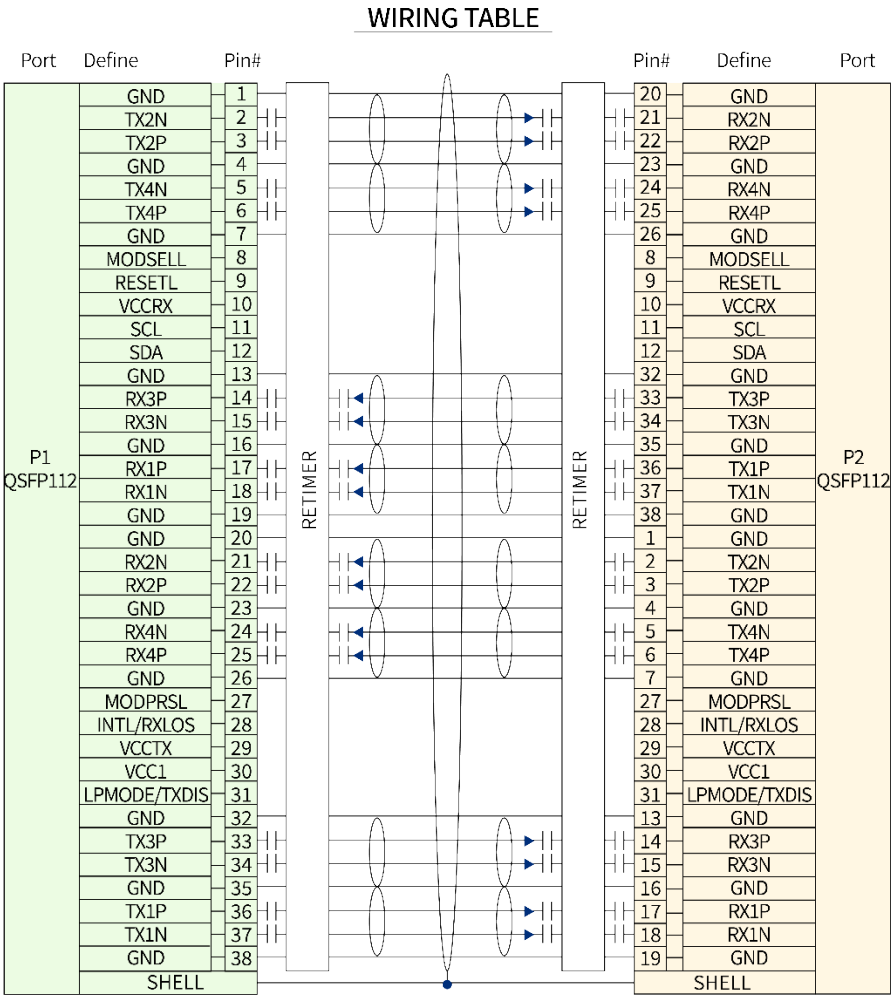


Figure 2 QSFP112 to QSFP112 400G AEC Wiring

2.10 Memory Map and Control Register (Compatible CMIS 5.x)

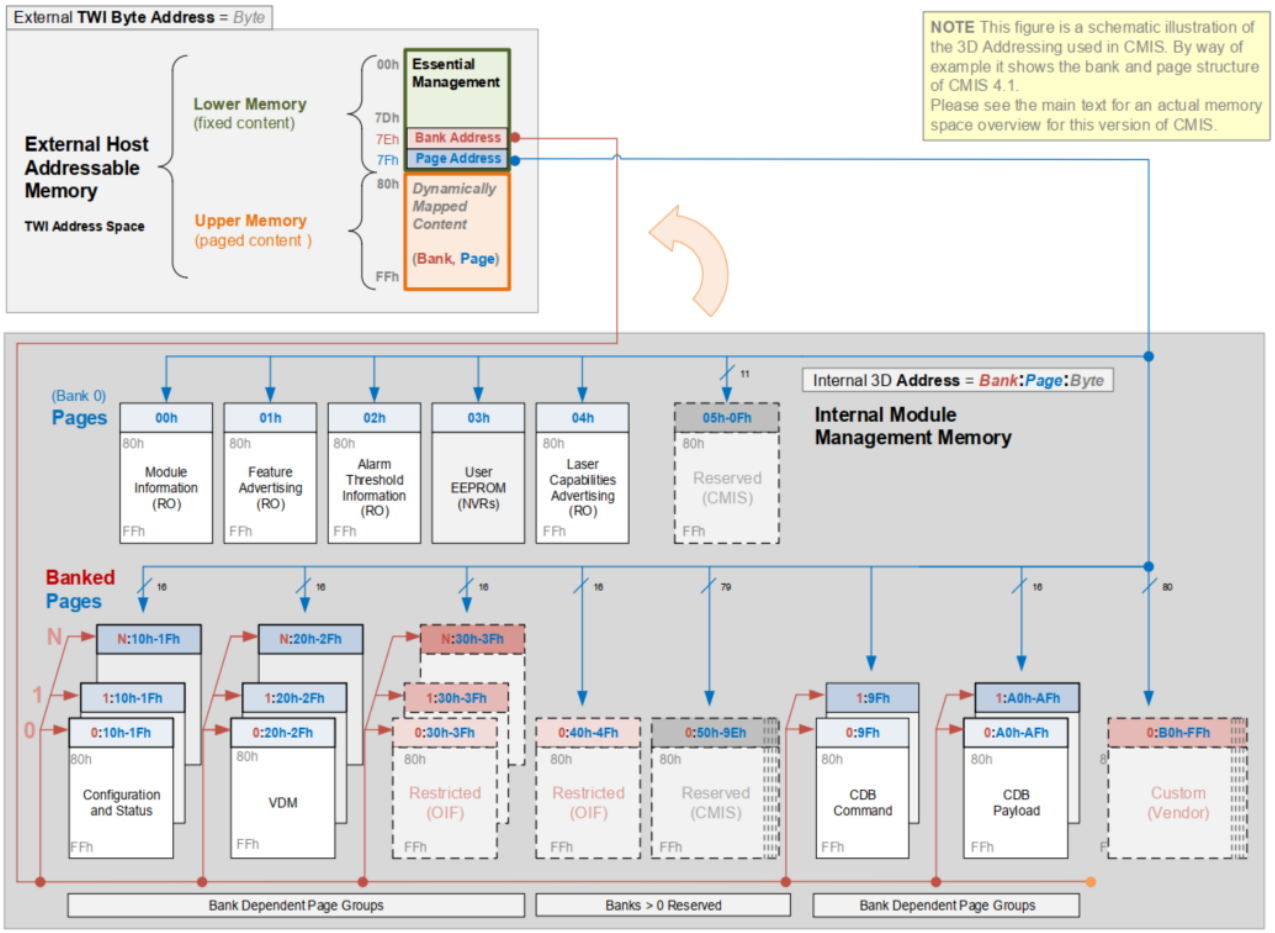


Figure 3 CMIS Module Memory Map (Conceptual View)

2.11 Mechanical Specifications

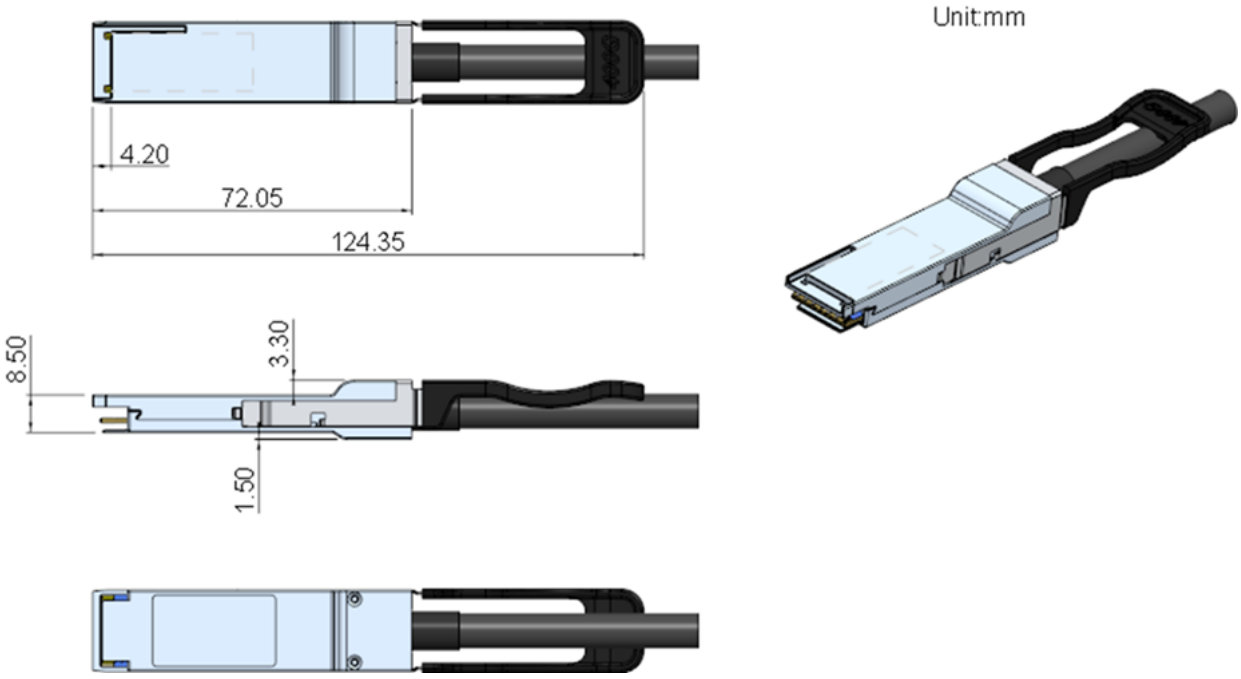
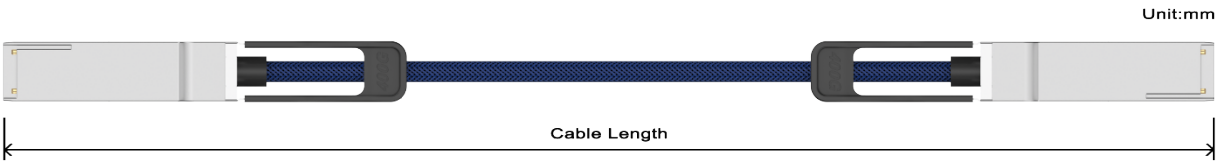


Figure 4 QSFP112 Form Factor

3.0 Product Information



Product ID	Product Description	Tolerance	AWG
Q112-Q112-400G-AEC-3210	QSFP112 to QSFP112 400G AEC w/ Marvell Lynx 400 DSP ,32AWG-1.0M	±30	32
Q112-Q112-400G-AEC-3215	QSFP112 to QSFP112 400G AEC w/ Marvell Lynx 400 DSP ,32AWG-1.5M	±40	32
Q112-Q112-400G-AEC-3220	QSFP112 to QSFP112 400G AEC w/ Marvell Lynx 400 DSP ,32AWG-2.0M	±40	32
Q112-Q112-400G-AEC-3225	QSFP112 to QSFP112 400G AEC w/ Marvell Lynx 400 DSP ,32AWG-2.5M	±50	32
Q112-Q112-400G-AEC-3030	QSFP112 to QSFP112 400G AEC w/ Marvell Lynx 400 DSP ,30AWG-3.0M	±50	30
Q112-Q112-400G-AEC-3035	QSFP112 to QSFP112 400G AEC w/ Marvell Lynx 400 DSP ,30AWG-3.5M	±60	30
Q112-Q112-400G-AEC-3040	QSFP112 to QSFP112 400G AEC w/ Marvell Lynx 400 DSP ,30AWG-4.0M	±60	30
Q112-Q112-400G-AEC-2850	QSFP112 to QSFP112 400G AEC w/ Marvell Lynx 400 DSP ,28AWG-5.0M	±70	28
Q112-Q112-400G-AEC-2860	QSFP112 to QSFP112 400G AEC w/ Marvell Lynx 400 DSP ,28AWG-6.0M	±80	28
Q112-Q112-400G-AEC-2870	QSFP112 to QSFP112 400G AEC w/ Marvell Lynx 400 DSP ,28AWG-7.0M	±90	28

Important Notice

The performance figures, data, and any illustrative material presented in this datasheet are typical and must be explicitly confirmed in writing by LINKPRO before they are deemed applicable to any specific order or contract.

By LINKPRO 's policy of continuous improvement, specifications may change without prior notice. The publication of information in this datasheet does not imply exemption from patent or other protective rights held by LINKPRO or other parties. Additional details can be obtained from any LINKPRO sales representative.

4.0 Revision Record

Rev.	Comments	Author	Date
A01	Initial Release	James Chen	08/07/2024
A02	Correct typo	James Chen	12/20/2024
A03	Corrected spelling errors	James Chen	12/21/2024
A04	Correct typos and Chang Jacket Color	James Chen	02/15/2025