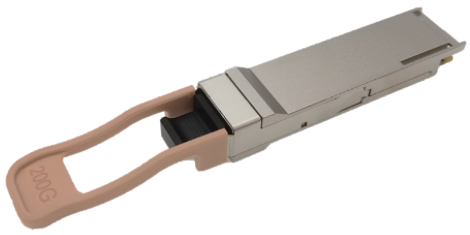
LPCRMM85-S10C

QSFP56 200Gb/s SR4 100m DDM

PRODUCT FEATURES

- Supports 212.5Gb/s aggregate bit rate
- 4x26.5625GBd(PAM4)electrical interface
- VCSEL Transmitter
- PIN and TIA array on the receiver side
- Maximum link length of 100m on OM4 Multimode Fiber (MMF)
- Hot-pluggable QSFP56 footprint
- Single MPO 12 receptacle
- Low power Consumption
- RoHS-6 compliant and lead-free
- +3.3V single power supply
- Support Digital Diagnostic Monitor interface
- Case operating temperature, Commercial: 0°C to +70°C



APPLICATIONS

- 200GBASE-SR4 200G Ethernet

Compliance

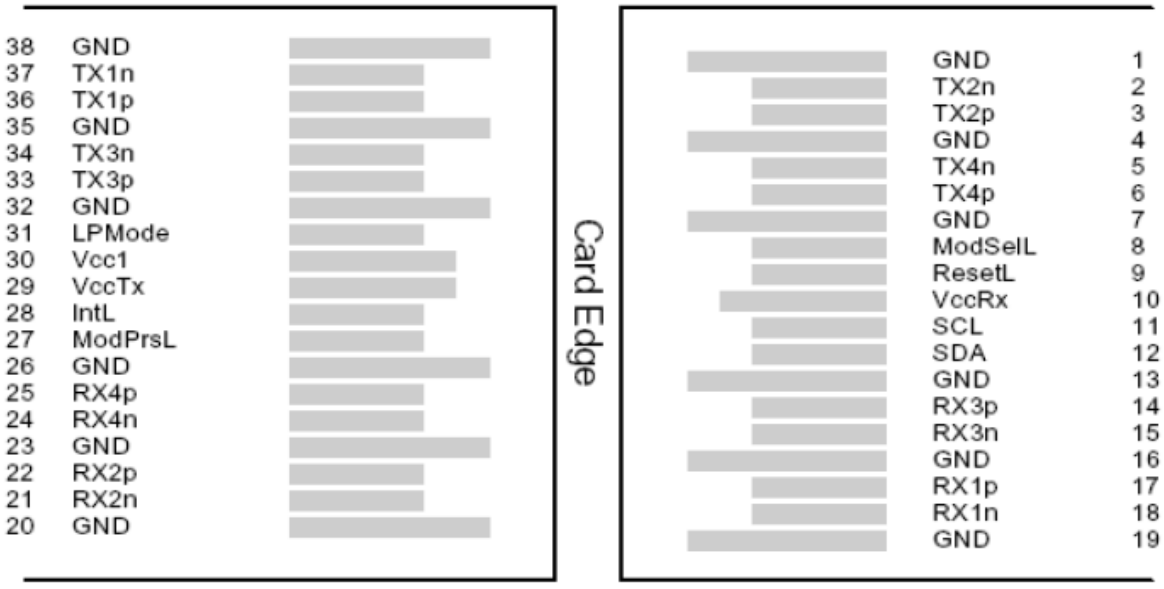
- QSFP MSA.
- IEEE802.3cd
- SFF-8636
- RoHS

Ordering information

Part NO.	Bit Rate (Gbps)	Laser (nm)	Distance(m)	Media	DDMI	Connector	Temp（℃）
LPCRMM85-S10C	212.5	850	100 (OM4)	multi-mode fiber	YES	MPO 1X12	0~70

LinkPro™

I. Pin Diagram



Top Side
Viewed from Top

Bottom Side
Viewed from Bottom

II. Pin Descriptions

Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSe1L	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		Vcc Rx	+3.3V Power supply receiver	
11	LVCMOS-I	SCL	2-wire serial interface clock	
12	LVCMOS-I/O	SDA	2-wire serial interface data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	

19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrSL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		Vcc Tx	+3.3V Power supply transmitter	
30		Vcc1	+3.3V Power Supply	
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1

Note：

1. Circuit ground is internally isolated from chassis ground.

III. Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Ref.
Storage Temperature	T_S	-40		85	ºC	
Storage Ambient Humidity	H_A	0		85	%	
Maximum Supply Voltage	V_{CC}	-0.5		3.6	V	

IV. Recommended Operating Conditions

Data Rate Spcifications	Symbol	Min.	Typ.	Max.	Unit	Ref.
Supply Voltage	Vcc	3.13	3.3	3.47	V	
Baud Rate(per channel) PAM4	BR		26.5625		GBd	1
Operating Case Temperature	Tc	0		70	℃	
Link distance on OM3 MMF	d			70	meters	
Link distance on OM4 MMF	d			100	meters	

Notes1. Supports 200GBASE-SR4 per IEEE 802.3cd.

V. Optical Characteristics

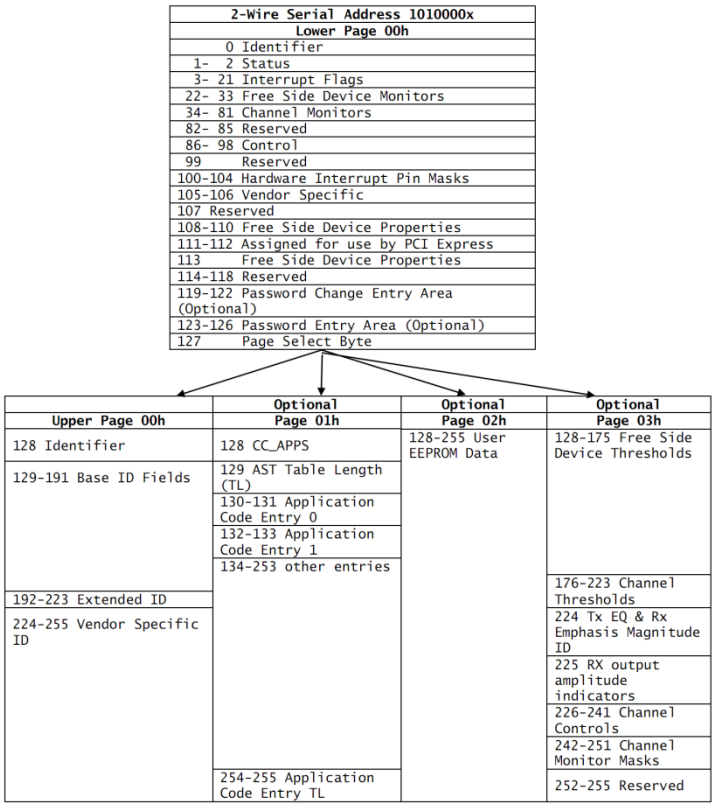
Parameter	Symbol	Min.	Typ.	Max.	Unit	Ref.
Transmitter(per lane)						
Average Output Power per lane	P_{OUT}	-6.5		4	dBm	
Outer Optical Modulation Amplitude per lane	OMA_{OUT}	-4.5		3	dBm	
Extinction Ratio	ER	3			dB	
Center Wavelength	λ_C	840		860	nm	
RMS Spectral Width	σ			0.6	nm	
Launch power in OMA_{OUT} minus TDECQ	P_{TDECQ}	-5.9			dBm	
Transmitter and dispersion eye closure (each lane)	TDECQ			4.5	dB	
Transmitter OFF Output Power	P_{Off}			-30	dBm	
Optical Return Loss Tolerance	ORLT			12	dB	
Receiver(per lane)						
Input Optical Wavelength	λ_{IN}	840		860	nm	
Average Recevive Power per lane	Pin	-8.4		4	dBm	
Receiver Power (OMA_{OUT}) each lane	R_{OMA}			3	dBm	
Rx Sensitivity(OMA_{OUT}) per lane (SECQ=1.4 dB)	R_{SENS}			-6.5	dBm	1
Stressed Rx Sensitivity(OMA) per lane	SR_{SENS}			-3	dBm	
Damage threshold	P_{DT}	5			dBm	
Receiver Reflectance	Rfl			-12	dBm	
LOS Assert	LOSA	-30			dBm	
LOS De-Assert	LOSD			-9	dBm	
LOS Hysteresis	LOSH	0.5			dB	

Note1. BER<2.4E-4,Pattern PRBS31Q.

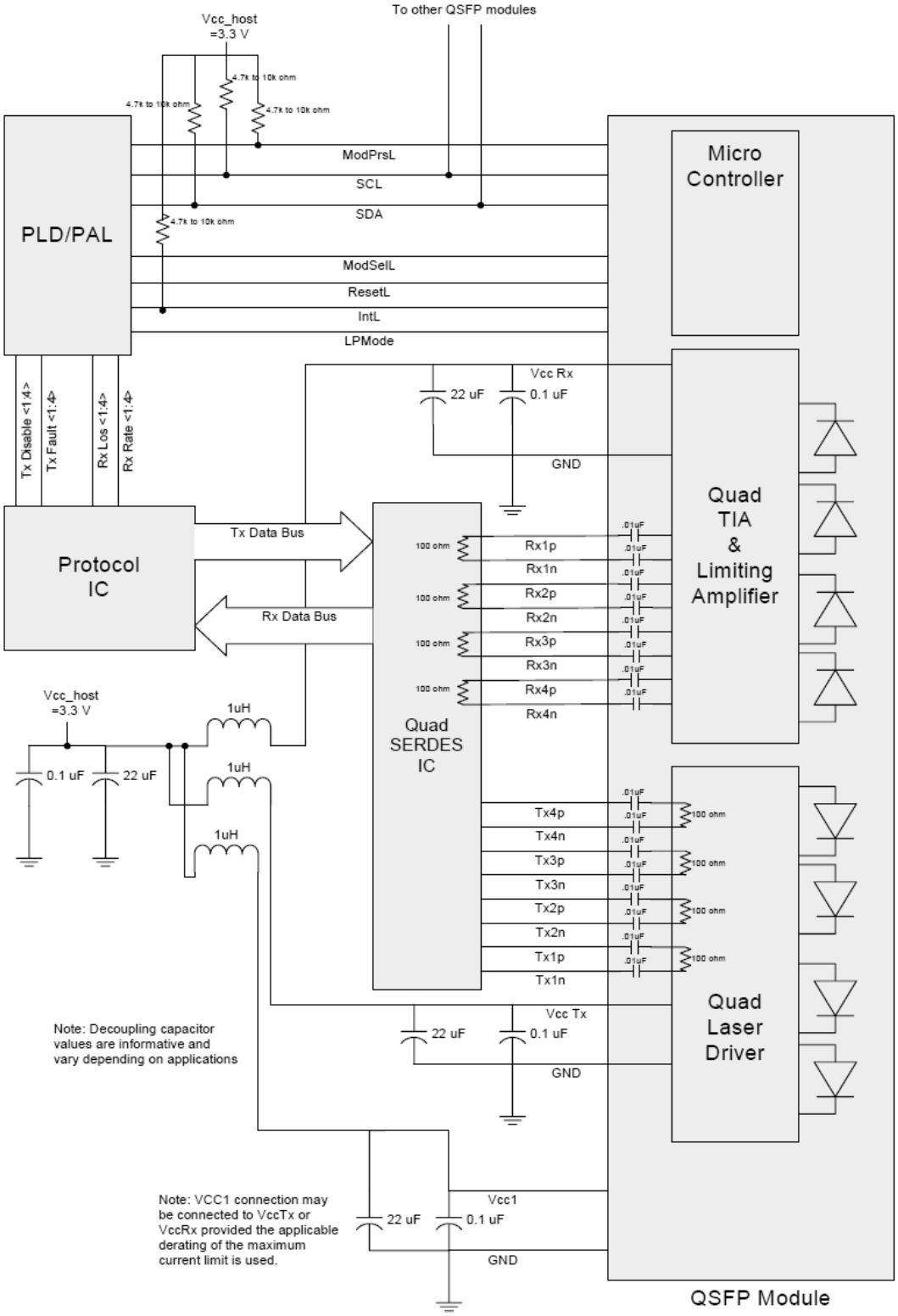
VI. Electrical Interface Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Ref.
Supply Voltage	V_{CC}	3.15		3.45	V	
Power Dissipation	Pd			6	W	
Transmitter(per Lane)						
Input different impedance	R_{in}	90	100	110	Ω	
Single ended input voltage tolerance	VinT	-0.3		4.0	V	
Differential Input Voltage Amplitude	$V_{in,pp}$			900	mV	
Receiver (per Lane)						
Error Bit Rate	BER			2.4E-4		
Output different impedance	R_{out}	90	100	110	Ω	
Single-ended output voltage	VoutR	-0.3		4.0	V	
Differential Output Voltage Amplitude	$V_{out,pp}$			900	mV	

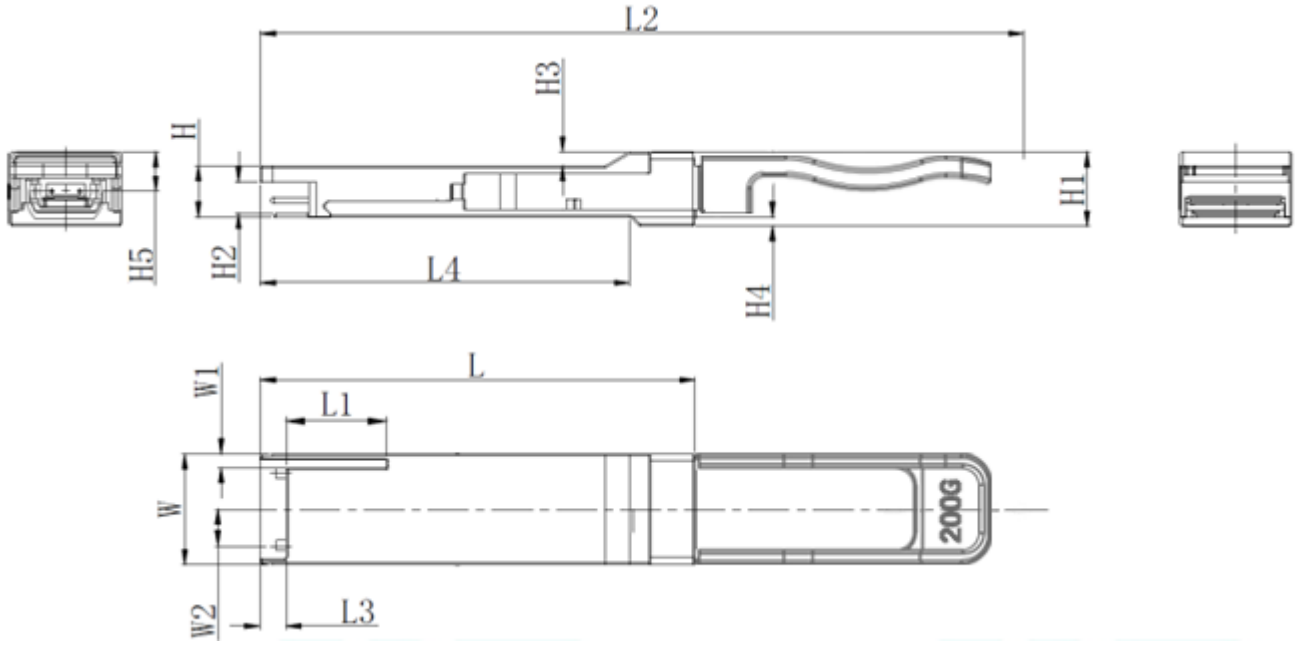
VII. Digital Diagnostic Functions



VIII.Recommended Interface Circuit



IX. Mechanical Specifications (Unit: mm)



Unit mm

	L	L1	L2	L3	L4	W	W1	W2	H	H1	H2	H3	H4	H5
Max	72.2	-	-	4.35	61.4	18.45	-	6.2	8.6	12.4	5.35	2.5	1.6	-
TYPE	72	-	121	4.2	61.2	18.35	-	-	8.5	12.2	5.2	2.3	1.5	6.55
Min	68.8	16.5	-	4.05	61	18.25	2.2	5.8	8.4	12	5.05	2.1	1.3	-